Access DB# _____

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: Justin King Examiner #: 79227 Date: 6-15-05
Art Unit: 2181 Phone Number 30 5-4571 Serial Number: 09/485 443
Mail Box and Bldg/Room Location: 2A08 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: _____

Inventors (please provide full names): _____

_____

Earliest Priority Filing Date: _____

For Sequence Searches Only *Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

Re Fouts 09/485,443

compare connection speeds, port count

Tree topology

****

STAFF USE ONLY	Type of Search	Vendors and cost where applicable
Searcher: C Wong	NA Sequence (#) _____	STN 4
Searcher Phone #: 305 9329	AA Sequence (#) _____	Dialog _____
Searcher Location: PK2-4B33	Structure (#) _____	Questel/Orbit _____
Date Searcher Picked Up: 6-19	Bibliographic _____	Dr.Link _____
Date Completed: 6-20	Litigation _____	Lexis/Nexis _____
Searcher Prep & Review Time: 45	Fulltext _____	Sequence Systems _____
Clerical Prep Time: _____	Patent Family _____	WWW/Internet _____
Online Time: _____	Other _____	Other (specify) _____

PTO-1590 (8-01)

STIC Search Report
EIC 2100

STIC Database Tracking Number: 51898

TO: Justin King **Location: 2A08** **Art Unit : 2181** **Friday, June 20, 2003** **Cas Serial Number: 09/485,443**	**From: Carol Wong** **Location: EIC 2100** **PK2-4B33** **Phone: 305-9729** **carol.wong@uspto.gov**

Search Notes

Dear Examiner King,

Attached are the search results (from commercial databases) for your case.

Color tags mark the patents/articles which appear to be most relevant to the case. As discussed, I used a different search strategy (comparing speeds and port count), which yielded different results. However, they don't appear to be relevant for your case. – sorry!

Please call if you have any questions or suggestions for additional terminology, or a different approach to searching the case.

Thanks,
Carol

```
File 347:JAPIO Oct 1976-2003/Feb(Updated 030603)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200338
         (c) 2003  Thomson Derwent
? ds

Set     Items   Description
S1     163894   TREE OR TREES OR HIERARCH? OR TREEMAP? OR GRID OR GRIDS OR
             TOPOLOG?????? ? OR PYRAMID? ? OR CASCAD? OR SUBTREE? ?
S2      88362   PARENT? ? OR CHILD OR CHILDREN
S3     983418   SPEED OR SPEEDS
S4       4304   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (PORT OR PORTS)
S5       2953   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (NODE OR NODES)
S6     280575   SPEEDIER OR SPEEDIEST OR CELERITY? OR RAPID OR RAPIDLY OR -
             RAPIDER OR RAPIDEST OR RAPIDITY OR RAPIDNESS OR SWIFT???? ?
S7     426397   FAST OR FASTER OR FASTEST OR FASTNESS OR QUICK???? ?
S8      35362   (S3 OR S6:S7)(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK???
              ? OR INTERLINK?)
S9       1125   S4:S5(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK??? ? OR I-
             NTERLINK?)
S10    864237   COMPAR?
S11     53781   S10(5N)(PORT OR PORTS OR NODE OR NODES OR S3 OR S6:S7 OR D-
             EVICE? ? OR BUS OR BUSSES OR BUSES)
S12     89452   S10(5N)(APPARATUS? OR APP?? ? OR NETWORK? ? OR COMPONENT? ?
              OR UNIT OR UNITS OR SYSTEM? ? OR MODULE? ? OR TERMINAL? ? OR
             COMPUTER? ? OR PC OR PCS)
S13      8349   S10(5N)(PCU? ? OR WORKSTATION? OR WORK()STATION? ? OR CPU?
             ? OR CONSOLE? ? OR CLIENT? ? OR MICROPROCESS?R? ? OR MICROCOM-
             PUT?)
S14      5873   SL:S2 AND S11:S13
S15      2223   S1:S2 AND S11:S13
S16        49   S14 AND S8
S17         3   S14 AND S9
S18      1584   1394
S19        20   S18 AND S4:S5
S20        19   S18 AND S8
S21        86   (S19:S20 OR S16) NOT S17
S22        86   IDPAT (sorted in duplicate/non-duplicate order)
S23        82   IDPAT (primary/non-duplicate records only)
? ds

Set     Items   Description
S1     163894   TREE OR TREES OR HIERARCH? OR TREEMAP? OR GRID OR GRIDS OR
             TOPOLOG?????? ? OR PYRAMID? ? OR CASCAD? OR SUBTREE? ?
S2      88362   PARENT? ? OR CHILD OR CHILDREN
S3     983418   SPEED OR SPEEDS
S4       4304   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (PORT OR PORTS)
S5       2953   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (NODE OR NODES)
S6     280575   SPEEDIER OR SPEEDIEST OR CELERITY? OR RAPID OR RAPIDLY OR -
             RAPIDER OR RAPIDEST OR RAPIDITY OR RAPIDNESS OR SWIFT???? ?
S7     426397   FAST OR FASTER OR FASTEST OR FASTNESS OR QUICK???? ?
S8      35362   (S3 OR S6:S7)(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK???
              ? OR INTERLINK?)
S9       1125   S4:S5(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK??? ? OR I-
             NTERLINK?)
S10    864237   COMPAR?
```

```
S11      53781   S10(5N)(PORT OR PORTS OR NODE OR NODES OR S3 OR S6:S7 OR D-
                 EVICE? ? OR BUS OR BUSSES OR BUSES)
S12      89452   S10(5N)(APPARATUS? OR APP?? ? OR NETWORK? ? OR COMPONENT? ?
                  OR UNIT OR UNITS OR SYSTEM? ? OR MODULE? ? OR TERMINAL? ? OR
                 COMPUTER? ? OR PC OR PCS)
S13       8349   S10(5N)(PCU? ? OR WORKSTATION? OR WORK()STATION? ? OR CPU?
                 ? OR CONSOLE? ? OR CLIENT? ? OR MICROPROCESS?R? ? OR MICROCOM-
                 PUT?)
S14       5873   SL:S2 AND S11:S13
S15       2223   S1:S2 AND S11:S13
S16         49   S14 AND S8
S17          3   S14 AND S9
S18       1584   1394
S19         20   S18 AND S4:S5
S20         19   S18 AND S8
S21         86   (S19:S20 OR S16) NOT S17
S22         86   IDPAT (sorted in duplicate/non-duplicate order)
S23         82   IDPAT (primary/non-duplicate records only)
```

17/9/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010921836 **Image available**
WPI Acc No: 1996-418787/199642
XRPX Acc No: N96-353037

Number management method for hub connection in communication network - involves responding master hub by transmitting of recognition signal comprising recognition number from slave hub on reception of exaggeration signal

Patent Assignee: MATSUSHITA ELECTRIC WORKS LTD (MATW)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8204745	A	19960809	JP 9510872	A	19950126	199642	B

Priority Applications (No Type Date): JP 9510872 A 19950126
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8204745	A		6	H04L-012/44	

Abstract (Basic): JP 8204745 A

The network management method involves providing multiple **slave** hubs (S1-S5) in a master hub (M). The **slave** hubs are connected to three ports (P1-P3) provided in the master hub by a cascade connection in increasing order. The connection of **slave** hubs in the network is managed by transmitting and receiving management information between master and **slave** hubs. The number of **slave** hubs connected to each port is stored in the master hub. The **ports** with higher **number** of hubs **connected** are selected.

The **connection number** of selected **ports** is **compared**0 with the maximum **connectable** number specified beforehand. If the connection number exceeds the specified value, an exaggeration signal is transmitted to the **slave** hubs. The **slave** hub on receiving the signal transmits the recognised signal comprising the recognised number to the motor hub.

ADVANTAGE - Manages **slave** hub connection effectively.

Dwg.1/5

Title Terms: NUMBER; MANAGEMENT; METHOD; HUB; CONNECT; COMMUNICATE; NETWORK ; RESPOND; MASTER; HUB; TRANSMIT; RECOGNISE; SIGNAL; COMPRISE; RECOGNISE; NUMBER; **SLAVE** ; HUB; RECEPTION; SIGNAL
Index Terms/Additional Words: LAN
Derwent Class: W01
International Patent Class (Main): H04L-012/44
File Segment: EPI
Manual Codes (EPI/S-X): W01-A06B3
?

23/9/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013492932 **Image available**
WPI Acc No: 2000-664875/200064
Related WPI Acc No: 2000-647163; 2000-647164; 2001-024378; 2001-389897; 2001-389905; 2001-390067; 2001-390068; 2001-441156; 2001-610940; 2002-048974; 2002-179272; 2002-239811; 2002-470145; 2002-506734; 2003-327752
XRPX Acc No: N00-492795
Ordering interconnect topology to form ring structure, the topology has a number of nodes where each node is connected to a bus and computes to the ring identifier
Patent Assignee: SONY ELECTRONICS INC (SONY)
Inventor: FAIRMAN B; HUNTER D; JAMES D V
Number of Countries: 091 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200057283	A1	20000928	WO 2000US7517	A	20000320	200064 B
AU 200040188	A	20001009	AU 200040188	A	20000320	200103

Priority Applications (No Type Date): US 2000531280 A 20000318; US 99125321 P 19990319; US 99130698 P 19990423; US 99137916 P 19990607; US 99144101 P 19990716; US 99150393 P 19990823; US 99155305 P 19990921; US 99158722 P 19991011; US 99167958 P 19991129; US 99170962 P 19991215; US 2000177077 P 20000119
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200057283	A1	E	57	G06F-013/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW

AU 200040188	A		G06F-013/00	Based on patent WO 200057283

Abstract (Basic): WO 200057283 A1

NOVELTY - The method where the **number** of **nodes** (1002-1010) are connected to a bus. Determining a self identifier for each node which is then mapped to a ring identifier for each node, in addition each node computes the ring identifier of one of its port-connected (1022) nodes as its topologically adjacent neighbor.

DETAILED DESCRIPTION - When mapping a physical identification value is assigned to each of the **number** of **nodes** and communicating with an adjacent neighbor using adjacent neighbor identifier. The ring identifier is initialized to zero and is incremented when the message packets are passed through a given port of each node.

INDEPENDENT CLAIMS are also included for the following: A method for circumscribing an interconnect topology, the topology has a **number** of **nodes** and a **number** of bus bridges, A system for ordering an interconnect topology, the topology has a **number** of **nodes** to form a ring structure, A system for circumscribing an interconnect topology, the topology has a **number** of **nodes** and a **number** of bus bridges, and A computer readable medium comprising program instructions for encoding a block of data.

USE - For ordering an interconnect topology to form a ring structure.

ADVANTAGE - Able to transfer to display different types of data at the same time by the use of the high **speed** bus system for **interconnect** .

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram for a next neighbor ordering topology.

Topology (1000)

Number of **nodes** (1002-1010)

Port(a) (1022)

pp; 57 DwgNo 7/19

Technology Focus:

TECHNOLOGY FOCUS - INDUSTRIAL STANDARDS - The bus conforms to IEEE **1394** standard serial bus implemented by IEEE std **1394** -1995, standard for a high performance serial bus.

Title Terms: ORDER; INTERCONNECT; TOPOLOGICAL; FORM; RING; STRUCTURE; TOPOLOGICAL; NUMBER; NODE; NODE; CONNECT; BUS; COMPUTATION; RING; IDENTIFY

Derwent Class: T01; W01

International Patent Class (Main): G06F-013/00

File Segment: EPI

Manual Codes (EPI/S-X): T01-H; W01-A06B2

```
File   2:INSPEC 1969-2003/Jun W2
         (c) 2003 Institution of Electrical Engineers
File   6:NTIS 1964-2003/Jun W3
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2003/Jun W2
         (c) 2003 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2003/Jun W3
         (c) 2003 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2003/May
         (c) 2003 ProQuest Info&Learning
File  65:Inside Conferences 1993-2003/Jun W3
         (c) 2003 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2003/Jun W3
         (c)2003 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2003/Jun W1
         (c) 2003 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/May
         (c) 2003 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2003/Jun 16
         (c) 2003 The Gale Group
File 144:Pascal 1973-2003/Jun W1
         (c) 2003 INIST/CNRS
File 202:Info. Sci. & Tech. Abs. 1966-2003/May 14
         (c) Information Today, Inc
File 233:Internet & Personal Comp. Abs. 1981-2003/May
         (c) 2003 Info. Today Inc.
File 266:FEDRIP 2003/Apr
        Comp & dist by NTIS, Intl Copyright All Rights Res
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 483:Newspaper Abs Daily 1986-2003/Jun 18
         (c) 2003 ProQuest Info&Learning
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
? ds

Set     Items   Description
S1    1335350   TREE OR TREES OR HIERARCH? OR TREEMAP? OR GRID OR GRIDS OR
            TOPOLOG?????? ? OR PYRAMID? ? OR CASCAD? OR SUBTREE? ?
S2    1675677   PARENT? ? OR CHILD OR CHILDREN
S3    1115370   SPEED OR SPEEDS
S4       1853   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
            (PORT OR PORTS)
S5      15880   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
            (NODE OR NODES)
S6    1225572   SPEEDIER OR SPEEDIEST OR CELERITY? OR RAPID OR RAPIDLY OR -
            RAPIDER OR RAPIDEST OR RAPIDITY OR RAPIDNESS OR SWIFT???? ?
S7    1417011   FAST OR FASTER OR FASTEST OR FASTNESS OR QUICK???? ?
S8      37169   (S3 OR S6:S7)(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK???
             ? OR INTERLINK?)
S9        890   S4:S5(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK??? ? OR I-
            NTERLINK?)
S10   6732520   COMPAR?
S11     59949   S10(5N)(PORT OR PORTS OR NODE OR NODES OR S3 OR S6:S7)
S12      3786   S1:S2 AND S11
S13        34   S12 AND S8
S14         4   S12 AND S9
S15     29523   S10(5N)(DEVICE? OR BUS OR BUSSES OR BUSSES)
S16    321589   S10(5N)(APPARATUS? OR APP?? ? OR NETWORK? ? OR COMPONENT? ?
            OR UNIT OR UNITS OR SYSTEM? ? OR MODULE? ? OR TERMINAL? ? OR
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             COMPUTER? ? OR PC OR PCS)
S17      8037   S10(5N)(PCU? ? OR WORKSTATION? OR WORK()STATION? ? OR CPU?
             ? OR CONSOLE? ? OR CLIENT? ? OR MICROPROCESS?R? ? OR MICROCOM-
             PUT?)
S18     19682   S1:S2 AND S15:S17
S19       105   S18 AND S8
? t14/7/3
```

14/7/3 (Item 1 from file: 35)

01540115 ORDER NO: AAD97-11818

RESOURCE PLACEMENT, DATA REARRANGEMENT, AND HAMILTONIAN CYCLES IN TORUS NETWORKS (MULTICOMPUTERS)

Author: BAE, MYUNG MUN
Degree: PH.D.
Year: 1996
Corporate Source/Institution: OREGON STATE UNIVERSITY (0172)
Source: VOLUME 57/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 7035. 108 PAGES

Many parallel machines, both commercial and experimental, have been/are being designed with toroidal **interconnection** networks. For a given **number** of **nodes** , the torus has a relatively larger diameter, but better cost/performance tradeoffs, such as higher channel bandwidth, and lower **node** degree, when **compared** to the hypercube. Thus, the torus is becoming a popular **topology** for the interconnection network of a high performance parallel computers.

In a multicomputer, the resources, such as I/O devices or software packages, are distributed over the networks. The first part of the thesis investigates efficient methods of distributing resources in a torus network. Three classes of placement methods are studied. They are (1) distant-t placement problem: in this case, any non-resource node is at a distance of at most t from some resource nodes, (2) j-adjacency problem: here, a non-resource node is adjacent to at least j resource nodes, and (3) generalized placement problem: a non-resource node must be a distance of at most t from at least j resource nodes.

This resource placement technique can be applied to allocating spare processors to provide fault-tolerance in the case of the processor failures. Some efficient spare processor placement methods and reconfiguration schemes in the case of processor failures are also described.

In a torus based parallel system, some algorithms give best performance if the data are distributed to processors numbered in Cartesian order; in some other cases, it is better to distribute the data to processors numbered in Gray code order. Since the placement patterns may be changed dynamically, it is essential to find efficient methods of rearranging the data from Gray code order to Cartesian order and vice versa. In the second part of the thesis, some efficient methods for data transfer from Cartesian order to radix order and vice versa are developed.

The last part of the thesis gives results on generating edge disjoint Hamiltonian cycles in k-ary n-cubes, hypercubes, and 2D tori. These edge disjoint cycles are quite useful for many communication algorithms.
?

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Set     Items   Description
S1    1335350   TREE OR TREES OR HIERARCH? OR TREEMAP? OR GRID OR GRIDS OR
            TOPOLOG?????? ? OR PYRAMID? ? OR CASCAD? OR SUBTREE? ?
S2    1675677   PARENT? ? OR CHILD OR CHILDREN
S3    1115370   SPEED OR SPEEDS
S4       1853   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
            (PORT OR PORTS)
S5      15880   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
            (NODE OR NODES)
S6    1225572   SPEEDIER OR SPEEDIEST OR CELERITY? OR RAPID OR RAPIDLY OR -
            RAPIDER OR RAPIDEST OR RAPIDITY OR RAPIDNESS OR SWIFT???? ?
S7    1417011   FAST OR FASTER OR FASTEST OR FASTNESS OR QUICK???? ?
S8      37169   (S3 OR S6:S7)(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK???
             ? OR INTERLINK?)
S9        890   S4:S5(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK??? ? OR I-
            NTERLINK?)
S10   6732520   COMPAR?
S11     89299   S10(5N)(PORT OR PORTS OR NODE OR NODES OR S3 OR S6:S7 OR D-
            EVICE? ? OR BUS OR BUSSES OR BUSES)
S12    321589   S10(5N)(APPARATUS? OR APP?? ? OR NETWORK? ? OR COMPONENT? ?
             OR UNIT OR UNITS OR SYSTEM? ? OR MODULE? ? OR TERMINAL? ? OR
            COMPUTER? ? OR PC OR PCS)
S13      8037   S10(5N)(PCU? ? OR WORKSTATION? OR WORK()STATION? ? OR CPU?
            ? OR CONSOLE? ? OR CLIENT? ? OR MICROPROCESS?R? ? OR MICROCOM-
            PUT?)
S14     23149   S1:S2 AND S11:S13
S15       134   S14 AND S8
S16        44   S14 AND S9
S17        11   S15:S16 AND BUSES
S18         9   RD (unique items)
S19       177   S15:S16
S20        60   S19/1999:2003
S21       117   S19 NOT S20
S22        79   RD (unique items)
S23        71   S22 NOT S17
S24        67   S23 NOT TURBINE?
```

24/7/23 (Item 23 from file: 2)
DIALOG(R)File 2:INSPEC

04358898 INSPEC Abstract Number: B9304-6150P-010
Title: Multi- link - speed **network** topology **design**
Author(s): Chang, P.-C.; Kermani, P.; Kershenbaum, A.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: Eleventh Annual International Phoenix Conference on Computers and Communications (Cat. No.92CH3129-4) p.299-306
Publisher: IEEE, New York, NY, USA
Publication Date: 1992 Country of Publication: USA xvi+782 pp.
ISBN: 0 7803 0605 8
Conference Sponsor: IEEE; Arizona State Univ.; Univ. Arizona
Conference Date: 1-3 April 1992 Conference Location: Scottsdale, AZ, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The authors consider the problem of selecting a link **topology** and sizing the link given a point-to-point traffic matrix and a cost matrix. Different **speed links** are permitted in the **topology** . An algorithm is presented for the solution to this problem, and its performance, both in terms of running time and the quality of the **networks** produced, is **compared** with that of an algorithm which only considers a single **speed link** . The new algorithm shows significant improvement, reducing cost by as much as 6% while increasing running time by only a constant factor. (8 Refs)
Subfile: B

24/7/25 (Item 25 from file: 2)
DIALOG(R)File 2:INSPEC

03814262 INSPEC Abstract Number: B91008169, C91015824
Title: Delay models and speed **improvement techniques for RC** tree interconnections **among small-geometry CMOS inverters**
Author(s): Wu, C.-Y.; Shiau, M.-C.
Author Affiliation: Dept. of Electron. Eng., Nat. Chiao-Tung Univ., Hsinchu, Taiwan
Journal: IEEE Journal of Solid-State Circuits vol.25, no.5 p. 1247-56
Publication Date: Oct. 1990 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
U.S. Copyright Clearance Center Code: 0018-9200/90/1000-1247$01.00
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: Physical delay models entirely based upon device equations for small-geometry CMOS inverters with RC **tree** interconnection **networks** are presented. Through extensive **comparisons** with SPICE simulation results, it is shown that the maximum relative error in delay-time calculations using the developed model is within 15% for 1.5- mu m CMOS inverters with RC **tree** interconnection networks. An experimental sizing program is constructed for **speed** improvement of **interconnection** lines and **trees** . In this program, given the size of the input logic gate and its driving interconnection resistances, capacitances, and structures, users can choose one of four speed-improvement techniques and determine the suitable sizes and/or number of drivers/repeaters for a minimum delay. The four speed-improvement techniques use minimum-size repeaters and **cascaded**

input drivers to reduce the interconnection delay. It is found that the required tapering factor in **cascaded** drivers is not the base of the natural logarithm, but a value in the range 4-8. Adding a small number of drivers/repeaters with large sizes reduces the interconnection delay more efficiently. (27 Refs)
Subfile: B C

24/7/41 (Item 3 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01529834 ORDER NO: AAD97-04234
CURRENT MODE INTERCONNECT FOR ON-CHIP AND INTER-CHIP (GALLIUM ARSENIDE)
Author: ZHANG, JOHNNY QI
Degree: PH.D.
Year: 1996
Corporate Source/Institution: UNIVERSITY OF CALIFORNIA, SANTA BARBARA (0035)
Source: VOLUME 57/09-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 5838. 174 PAGES

The existing high **speed interconnects hierarchy** is reviewed. The importance of the **interconnects** in high **speed** systems is explored. A **comparative** study of the present high **speed interconnections** is presented. From both theoretical analysis and design, the current mode interconnects are shown to provide better performance either in speed or in power. For the on-chip **interconnect** , the current mode **interconnect** is **faster** with large loading capacitance. For interchip interconnect, the GaAs test chips have shown an operating speed of 1.2GHz with only 4.4mW power dissipation, demonstrating the power reduction by a factor of 8 compared with ECL interconnect. The CMOS interchip interconnect test chips consume only 2.5mW of power at 500MHz. The applications of the current mode interconnections are extended to multiple valued logic interconnect where ternary signals instead of binary signals are transferred. The current mode ternary interconnect can reduce wiring by half for serial interfaces and can eliminate clock skew problems while still keeping the low power dissipation. The current mode MVL test chips show the data transfer speed of 735MHz with 14mW power dissipation. The GaAs version of current mode interconnects is fabricated by Vitesse Semiconductor. The CMOS version of current mode interconnects is designed at AT&T Bell Labs for AT&T MBIC3 0.5 μm process.
?

24/7/42 (Item 4 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

824674 ORDER NO: AAD83-24050
PERFORMANCE BASED DESIGN AND ANALYSIS OF MULTIMICROCOMPUTER NETWORKS
Author: REED, DANIEL ALLEN
Degree: PH.D.
Year: 1983
Corporate Source/Institution: PURDUE UNIVERSITY (0183)
Source: VOLUME 44/06-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 1893. 311 PAGES

A new paradigm for parallel computation based on large numbers of interconnected microcomputer nodes has recently emerged. Each network node, fabricated as one or two VLSI chips would contain a processor with some local memory, a communication controller that routes messages without delaying the processor, and a few connections to other network nodes. The cooperating tasks of a parallel algorithm would execute asynchronously on different nodes and communicate via message passing. This approach to parallel processing poses several new and interesting problems in network performance evaluation, distributed task scheduling, and parallel algorithm design.

The absence of shared memory makes the evaluation and design of an interconnection network capable of efficiently supporting internode communication patterns crucial. A network model based on the asymptotic properties of closed queueing networks representing the effects of the network **topology** , node and communication **link speeds** , and the internode communication patterns is developed. With this model, it is possible to **compare** the performance of different **network topologies** processing the same workload, determine the range of network sizes over which a given **topology** can meet specified performance requirements, and calculate the size of computation quanta below which communication delays negate possible gains due to increased parallelism.

Because of communication delays, no node can possess an exact description of the entire network state; all scheduling decisions must be made using incomplete and possibly inaccurate status information. The efficacy of distributed scheduling heuristics as a function of network **topology** , status information accuracy, and the amount of computation represented by each task are examined. Knowledge of a small area surrounding each node is shown to be sufficient to make acceptable scheduling decisions.

Finally, the importance of partial differential equations as models of many phenomena has motivated the search for solution algorithms suited to multimicrocomputer networks. This work has sought to relax the severe synchronization constraints imposed by most algorithms and to determine an appropriate number of discretization points to place in each network node. This has led to a class of solution algorithms spanning the spectrum from completely sequential and synchronous to completely parallel and fully asynchronous.

?

1/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03984022 INSPEC Abstract Number: C91063564
Title: A comparison of homogeneous hierarchical interconnection **structures**
Author(s): Cantoni, V.; Ferretti, M.; Lombardi, L.
Author Affiliation: Dipartimento di Inf. e Sistemistica, Pavia Univ., Italy
Journal: Proceedings of the IEEE vol.79, no.4 p.416-28
Publication Date: April 1991 Country of Publication: USA
CODEN: IEEPAD ISSN: 0018-9219
U.S. Copyright Clearance Center Code: 0018-9219/91/0400-0416$01.00
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Among the various proposal advanced to build massive parallel systems in which the number of computing units ranges in the thousands, hierarchical topologies share a number of interesting properties. The authors review these architectures and their applicability and reliability, with particular attention to connections complexity and the ability to exchange messages. The usual assumption of the multiple instruction multiple data (MIMD) computational paradigm is as follows: autonomous but cooperating tasks execute on different processing units in the system. The overall complexity of the systems is measured with the analysis of the diameter and of the increasing law that states the number of interconnections against the number of nodes in the system. The various architectures are compared in terms of links load and average internode distance. (41 Refs)
Subfile: C
Descriptors: multiprocessor interconnection networks; parallel processing ; performance evaluation
Identifiers: MIMD computational paradigm; homogeneous hierarchical interconnection structures; massive parallel systems; reliability; connections complexity; links load; average internode distance
Class Codes: C4230 (Switching theory); C5440 (Multiprocessor systems and techniques); C5470 (Performance evaluation and testing)

2/7/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03966476 INSPEC Abstract Number: C91058180
Title: Hierarchical multi - microcomputer **systems**
Author(s): Cantoni, V.; Lombardi, L.; Ferretti, M.
Author Affiliation: Dipartimento di Inf. e Sistemistica, Pavia Univ., Italy
Conference Title: Proceedings. 10th International Conference on Pattern Recognition (Cat. No.90CH2898-5) p.476-8 vol.2
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1990 Country of Publication: USA 2 vol. (xxxi+xxv+1676) pp.
ISBN: 0 8186 2062 5
U.S. Copyright Clearance Center Code: CH2898-5/90/0000-0476$01.00
Conference Sponsor: Int. Assoc. Pattern Recognition
Conference Date: 16-21 June 1990 Conference Location: Atlantic City, NJ, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Hierarchical multi-microcomputer systems are reviewed, with particular attention given to the complexity of the interconnection structure and to the ability to exchange messages. The assumption of the multiple-instruction multiple-data (MIMD) computational paradigm is followed; autonomous but cooperating tasks execute on different processing units in the system. The overall complexity of the systems is measured with the analysis of the diameter and of the increasing law, which states the number of interconnections against the number of nodes in the system. The various architectures are compared in terms of links load and average internode distance under the uniform reference model of message distribution and of request independence assumption. (15 Refs)
Subfile: C

3/7/1 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

0079856 NTIS Accession Number: AD-603 165/XAB
Investigation of Propagation-Limited Computer Networks
(Final rept)
Elspas, B. ; Short, R. A. ; Goldberg, J. ; Stone, H. S. ; Minnick, R. C.
Stanford Research Inst Menlo Park Calif
Corp. Source Codes: 888888888
Report No.: AFCRL-64 376
Apr 64 2p
Journal Announcement: USGRDR6501

NTIS Prices: PC A02
Contract No.: AF19 628 2902; 4641; 4523; 464101
This report summarizes research on techniques for the logical analysis and design of computer networks in which the propagation delays on the lines connecting logic blocks within the network are appreciable compared to the delays within the blocks. The first part is concerned with basic techniques for the transfer of information between blocks. The problem of preserving the separation of pulses propagating in a cascade of delay elements is shown to be fundamental. For a cascade in which information flows in only one direction, through stages whose delays vary randomly and independently in time, preservation of pulse separation on a cascade of infinite length is shown to be impossible. A method for compensation of delays (which removes their independence) is proposed, but proof of its stability is incomplete. The second part is concerned with communication in large systems, and with special logical arrays. An analogy is made between propagation-limited networks and topological graphs, and the **relation between graph size** (number of nodes) and maximum distance (number of connecting branches in the shortest path) between nodes, is analyzed.

4/7/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02978171 E.I. Monthly No: EI9011136170
Title: Transportation-network design problem. Application of a hierarchical search algorithm.
Author: Chan, Yupo; Shen, T. Steven; Mahaba, Nizar M.
Corporate Source: Air Force Inst of Technology, OH, USA
Source: Transportation Research Record n 1251 1989 p 24-34
Publication Year: 1989
CODEN: TRREDM ISSN: 0361-1981
Language: English
Document Type: RC; (Report Chapter) Treatment: T; (Theoretical)
Journal Announcement: 9011
Abstract: Two variants of a network design problem are solved by application of the tree search method. The first formulation aims to reduce a specified vehicle-minutes of traffic congestion at the least possible budget expenditure, and the second minimizes traffic congestion for a given budget. Both involve system-optimizing traffic assignment models with multipath flows. The solution method consists of network abstraction, tree search, and network disaggregation - collectively referred to as the 'hierarchical search algorithm.' It is shown that such an algorithm reduces the search space by reducing the **number** of **nodes** and **links** and providing a tighter bound during the **tree** search. It also groups detailed links according to the function they perform - whether it be access/egress, line-haul, bypass, or internal circulation. However, the algorithm yields only a suboptimal solution, the quality of which is measured by an error function. The metropolitan network of Taipei, Taiwan, Republic of China, is used as a case study to verify some of the algorithmic properties, confirming its role in real-world applications. Finally, the performance of the algorithm, which is based on network abstraction, is favorably **compared** with a network-extraction network-design model. (Author abstract) 22 Refs.

5/K/1 (Item 1 from file: 95)
DIALOG(R)File 95:(c) 2003 FIZ TECHNIK. All rts. reserv.

ABSTRACT:
The authors analyze the reliability of three Fiber Distributed Data Interface (FDDI) **network topologies** and make **comparisons** . The three interconnection topologies considered are a tree, a double ring, and a ring of...

...reliability as a function of the stations' positions. They use the expressions to optimize the **number** of **ports** in and the topological interconnections of the wiring concentrators in order to achieve highest reliability...
? t5/7

5/7/1 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management
(c) 2003 FIZ TECHNIK. All rts. reserv.

00739030 E94016111021
A reliability analysis of failsoft FDDI networks
(Eine Zuverlaessigkeitsanalyse fehlertoleranter FDDI-Netze)
Jiahnsheng Yin; Silio, CBjun
Univ. of Maryland, College Park, USA; NRC Assoc., Aberdeen Proving Ground, USA
17th Conf. on Local Computer Networks, Minneapolis, USA, Sep 13-16, 1992
1992
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 0-8186-3095-7

ABSTRACT:
The authors analyze the reliability of three Fiber Distributed Data Interface (FDDI) **network topologies** and make **comparisons** . The three interconnection topologies considered are a tree, a double ring, and a ring of trees. The reliability measure is terminal-pair reliability in which the authors calculate the probability P(h(s,t)) that two arbitrarily positioned terminal stations (s and t) can communicate with each other. For the three FDDI network topologies considered they derive closed form expressions for P(h(s,t)) in terms of the failure probabilities of nodes, links, and network ports, and they also derive expressions for worst case reliability as a function of the stations' positions. They use the expressions to optimize the **number** of **ports** in and the topological interconnections of the wiring concentrators in order to achieve highest reliability for a given number of stations.
?

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File 348:EUROPEAN PATENTS 1978-2003/Jun W03
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030612,UT=20030605
         (c) 2003 WIPO/Univentio
? ds

Set     Items   Description
S1     150887   TREE OR TREES OR HIERARCH? OR TREEMAP? OR GRID OR GRIDS OR
             TOPOLOG?????? ? OR PYRAMID? ? OR CASCAD? OR SUBTREE? ?
S2      71025   PARENT? ? OR CHILD OR CHILDREN
S3     351112   SPEED OR SPEEDS
S4       7735   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (PORT OR PORTS)
S5       6320   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (NODE OR NODES)
S6     278052   SPEEDIER OR SPEEDIEST OR CELERITY? OR RAPID OR RAPIDLY OR -
             RAPIDER OR RAPIDEST OR RAPIDITY OR RAPIDNESS OR SWIFT???? ?
S7     346483   FAST OR FASTER OR FASTEST OR FASTNESS OR QUICK???? ?
S8      31801   (S3 OR S6:S7)(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK???
              ? OR INTERLINK?)
S9       2166   S4:S5(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK??? ? OR I-
             NTERLINK?)
S10    678583   COMPAR?
S11     53973   S10(5N)(PORT OR PORTS OR NODE OR NODES OR S3 OR S6:S7 OR D-
             EVICE? ? OR BUS OR BUSSES OR BUSES)
S12    101635   S10(5N)(APPARATUS? OR APP?? ? OR NETWORK? ? OR COMPONENT? ?
              OR UNIT OR UNITS OR SYSTEM? ? OR MODULE? ? OR TERMINAL? ? OR
             COMPUTER? ? OR PC OR PCS)
S13      7773   S10(5N)(PCU? ? OR WORKSTATION? OR WORK()STATION? ? OR CPU?
             ? OR CONSOLE? ? OR CLIENT? ? OR MICROPROCESS?R? ? OR MICROCOM-
             PUT?)
S14      3073   S1:S2(S)S11:S13
S15        82   S14(S)S8
S16        20   S14(S)S9
S17        15   S15/TI,AB,CM
S18       403   S1:S2(20N)S8
S19        11   S18(S)S11:S13
S20       202   S1:S2(15N)S9
S21        13   S20(S)S11:S13
S22    106646   IC='G06F'
S23     48910   IC='H04L'
S24        52   S15 AND S22:S23
S25        68   S19 OR S21 OR S24
S26        46   S25 NOT S16:S17
S27      5043   1394
S28      2012   S27 AND S3:S4
S29       661   S27(S)S3:S4
S30       500   S27(S)SERIAL(S)S3:S4
S31        16   S27(20N)S9
S32        15   S31 NOT (S16:S17 OR S26)
S33       636   S8(15N)S10
S34         1   S33(S)S27
S35         1   S34 NOT (S16:S17 OR S26 OR S32)
S36         1   S27(20N)S8(20N)S10
S37       130   S27(20N)S8
S38         1   S37(20N)S10
S39        15   S37(20N)S1:S2
S40        14   S38:S39 NOT (S16:S17 OR S26 OR S32 OR S36)
```

16/5,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00599381

A packet-switching communication network and method of design.
Paketvermittlungskommunikationsnetz und Verfahren zu seinem Entwurf.
Reseau de communication de commutation par paquets et methode de conception a cet effet.

PATENT ASSIGNEE:
MITA INDUSTRIAL CO., LTD., (283522), 2-28, 1-chome, Tamatsukuri Chuo-ku, Osaka 540, (JP), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
Sugano, Masashi, c/o Mita Ind. Co.,Ltd. 2-28 Tamatsukuri,1-ch., Chuo-ku Osaka 540, (JP)
Miyahara, Hideo, 4-7, Hagoromo-cho, Nishinomiya-shi,, Hyogo-ken, (JP)
Murata, Masayuki, 5-7-1, Kasuga-cho, Toyonaka-shi, Osaka, (JP)
LEGAL REPRESENTATIVE:
Cheyne, John Robert Alexander Mackenzie et al (41272), HASELTINE LAKE & CO. 28 Southampton Buildings Chancery Lane, London WC2A 1AT, (GB)
PATENT (CC, No, Kind, Date): EP 579472 A2 940119 (Basic)
EP 579472 A3 940817
APPLICATION (CC, No, Date): EP 93305460 930713;
PRIORITY (CC, No, Date): JP 92187132 920714; JP 92246918 920916
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: H04L-012/56; H04Q-011/04;

ABSTRACT EP 579472 A2
A communication network and method of design thereof uses end-to-end delay distribution functions and loss probabilities as design constraint to ensure that all packets of all traffic classes on all end-to-end node pairs of the network reach a destination within a predetermined maximum allowable delay with a given probability. An end-to-end delay distribution function is determined for every end-to-end path for all traffic classes to find a path with a minimum distribution probability value. A distribution function is determined for each link of the path having a minimum distribution probability value to determine a most congested link, the capacity of which is increased until a given minimum probability value of distribution is determined. (see image in original document)
ABSTRACT WORD COUNT: 120

LEGAL STATUS (Type, Pub Date, Kind, Text):

Refusal:	20000216	A2	Date European patent application was refused: 19991001
Application:	940119	A2	Published application (A1with Search Report ;A2without Search Report)
Change:	940406	A2	Inventor (change)
Change:	940720	A2	Obligatory supplementary classification (change)
Search Report:	940817	A3	Separate publication of the European or International search report
Change:	941102	A2	Representative (change)
Examination:	950215	A2	Date of filing of request for examination: 941216
Examination:	971229	A2	Date of despatch of first examination report: 971110

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	3204
SPEC A	(English)	EPABF2	10054
Total word count - document A			13258
Total word count - document B			0
Total word count - documents A + B			13258

...SPECIFICATION until ultimately the conditions of step S4 are satisfied.
Example 1
An example which provides **comparative** results between conventional methods of **network** design and that of the present invention will now be described with reference to Figure...

...e.g., predetermined by a uses and input to the CPU 2).
The number of **links** m = 7, and the **number** of **nodes** n = 4.
The **topology** of the network is as shown in Figure 2.
The routing matrix of the network...in the flow chart 15' are obtained.
Example 3
A description of an example illustrating **comparative** results between conventional methods of **network** design and that of the present invention is provided with reference to Figure 2 and...

...following values are initially given (e.g., predetermined).
Regarding the network 10:
The number of **links** m = 7, and the **number** of **nodes** n = 4. The **topology** of the network is as shown in Figure 2. The routing matrix of the network...

16/5,K/8 (Item 8 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00546532
Telecommunication switching system having adaptive routing switching nodes
Fernmeldevermittlungssystem mit adaptativen Leitweglenkungsvermittlungschalter
Systemede commutation pour telecommunicationavec des noeuds de commutation d'acheminement adaptatif
PATENT ASSIGNEE:
AT&T Corp., (589370), 32 Avenue of the Americas, New York, NY 10013-2412, (US), (Proprietor designated states: all)
INVENTOR:
Bales, Bruce Merrill, 493 Muirfield Court, Louisville, Colorado 80027, (US)
Crumpley, Robert Louis, 11837 West 108th Drive, Broomfield, Colorado 80021, (US)
North, Sandra Sue, 278 Pine Road, Golden, Colorado 80403, (US)
Thieler, Stephen Max, 4465 Apple Way, Boulder, Colorado 80301, (US)
LEGAL REPRESENTATIVE:
Williams, David John et al (86433); Page White & Farrer, 54 Doughty Street, London WC1N 2LS, (GB)
PATENT (CC, No, Kind, Date): EP 556515 A2 930825 (Basic)
EP 556515 A3 941207
EP 556515 B1 020626
APPLICATION (CC, No, Date): EP 92311267 921210;
PRIORITY (CC, No, Date): US 816362 911230
DESIGNATED STATES: DE; ES; FR; GB; IT
INTERNATIONAL PATENT CLASS: H04Q-003/00; H04Q-003/66

CITED PATENTS (EP B): EP 167951 A; EP 550178 A; EP 550179 A; EP 550180 A; EP 550181 A; DE 3632827 A; DE 3921637 A

CITED REFERENCES (EP B):

IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, vol.7, no.3, April 1989, NEWYORK (US), XP31235 MURAKAMI ET AL 'Control Architecture for Next-Generation Communication Networks Based on Distributed Databases'

L'ONDE ELECTRIQUE, vol.71, no.5, 9 October 1991, PARIS (FR) pages 49 - 53, XP263122 SEVEQUE ET AL 'ABC - A state-of-the-art private networking solution';

ABSTRACT EP 556515 A2

A telecommunication switching system having switching nodes that perform adaptive routing by utilizing the fact that the switching nodes are arranged in a first and a second hierarchy. In addition, each switching node maintains routing information based on telephone and switching node numbers which identify the switching nodes. A destination switching node transfers its routing information back to an originating switching node which combines that routing information with its own in order to determine shorter call paths for subsequent call routing. The first hierarchy is a dialing plan hierarchy having groups of switching nodes at each dialing plan level. The second hierarchy is a switching node hierarchy based on the switching node number of each switching node with at least one switching node of the switching node hierarchy being at a different level in the dialing plan hierarchy. In order to route a call, a switching node first routes through levels of switching nodes in the dialing plan hierarchy until a second switching node is encountered which can determine the identification of the destination switching node based on a dialed telephone number. The second switching node then routes the call through the node hierarchy using the identified node number until a path is determined to the destination switching node. (see image in original document)

ABSTRACT WORD COUNT: 216

NOTE:

Figure number on first page: 2

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	000913	A2	Date of dispatch of the first examination report: 20000726
Application:	930825	A2	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	030618	B1	No opposition filed: 20030327
Change:	010117	A2	Legal representative(s) changed 20001128
Grant:	020626	B1	Granted patent
*Assignee:	940622	A2	Applicant (name, address) (change)
*Assignee:	941005	A2	Applicant (transfer of rights) (change): AT&T Corp. (589370) 32 Avenue of the Americas New York, NY 10013-2412 (US) (applicant designated states: DE;ES;FR;GB;IT)
Search Report:	941207	A3	Separate publication of the European or International search report
Examination:	950726	A2	Date of filing of request for examination: 950524

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1353
CLAIMS B	(English)	200226	1496
CLAIMS B	(German)	200226	1292
CLAIMS B	(French)	200226	1836
SPEC A	(English)	EPABF1	25250
SPEC B	(English)	200226	25282

Total word count - document A 26606
Total word count - document B 29906
Total word count - documents A + B 56512

...SPECIFICATION REQUEST 1506, entity 2001 uses the **node number** received in **LINK** ...

...determine the network and the user destinations. Before the transmission of primitive 1506, entity 2001 **compares** the **node** numbers and from this **comparison** determines which of the entities will be defined the user or the network. For other...

...SPECIFICATION unidentified entity.
In forming the DL(underscore)ESTABLISH(underscore)REQUEST 1506, entity 2001 uses the **node number** received in **LINK** (underscore)AVAIL 1511 primitive to determine the position of the new node within the node **hierarchy** . As previously mentioned, each node has a unique node number, and the number itself determines the position within the node **hierarchy** . In addition, this information is utilized to decide which entity is going to be the...

...determine the network and the user destinations. Before the transmission of primitive 1506, entity 2001 **compares** the **node** numbers and from this **comparison** determines which of the entities will be defined the user or the network. For other...

26/5,K/27 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00897837 **Image available**
SPANNING TREE ALTERNATE ROUTING BRIDGE PROTOCOL
PROTOCOLE DE PONT POUR ACHEMINEMENT DETOURNE AVEC ARBRE MAXIMAL
Patent Applicant/Assignee:
GENERAL INSTRUMENT CORPORATION, 101 Tournament Drive, Horsham, PA 19044, US, US (Residence), US (Nationality)
Inventor(s):
LUI King-Shan, 1107 W. Gran Street, Urbana, IL 61801, US,
LEE Whay Chiou, 16 Michael Way, Cambridge, MA 02141, US,
Legal Representative:
VOLPE Anthony S (et al) (agent), Volpe and Koenig, P.C., Suite 400, One Penn Center, 1617 John F. Kennedy Boulevard, Philadelphia, PA 19103, US ,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200232058 A2-A3 20020418 (WO 0232058)
Application: WO 2001US42762 20011013 (PCT/WO US0142762)
Priority Application: US 2000239842 20001013
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **H04L-012/28**
International Patent Class: **H04L-012/46**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 22096

English Abstract
Bridges (10, 12, 14) are used to interconnect local area networks transparently. In the IEEE 802.1D standard for bridges, a spanning tree is built among the bridges for loop-free frame forwarding (FIG. 10). Although this approach is simple, it does not support all-pair shortest paths. A novel bridge protocol is employed that attempts to find and forward frames over alternate paths that are shorter than their corresponding tree paths on the standard spanning tree, and makes use of the standard spanning tree for default forwarding. The proposed protocol, referred to as the Spanning Tree Alternate Routing (START) Bridge Protocol, is backward compatible with the IEEE 802.1D standard and has a complexity that is comparable to that of the standard and other existing protocols.

French Abstract
Des ponts (10, 12, 14) sont utilises pour interconnecter des reseaux locaux de maniere transparente. Selon la norme IEEE 802.1D relative aux ponts, un arbre maximal est mis en place parmi les ponts pour la retransmission de trames sans boucle (FIG. 10). En depit de sa simplicite, cette approche ne peut etre appliquee pour les chemins les plus courts parmi toutes les paires possibles. Selon l'invention, on emploie un nouveau protocole de pont qui cherche a trouver et a acheminer

des trames par des chemins detournes qui sont plus courts que leurs chemins correspondants sur l'arbre maximal standard. Ce nouveau protocole fait appel a l'arbre maximal standard pour la retransmission par defaut. Le protocole propose, appele protocole de pont pour acheminement detourne avec arbre maximal (START), est retrocompatible avec la norme IEEE 802.1D et presente une complexite comparable a celle des protocoles standard et des autres protocoles existants.

Legal Status (Type, Date, Text)
Publication 20020418 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20020808 Late publication of international search report
Republication 20020808 A3 With international search report.
Examination 20021205 Request for preliminary examination prior to end of 19th month from priority date

Main International Patent Class: **H04L-012/28**
International Patent Class: **H04L-012/46**
Fulltext Availability:
Detailed Description

Detailed Description
... address certain shortcoming of the IDLS method. Specifically, Perlman, et al., proposed to identify non- **tree** links so that they can be used for forwarding frames without traveling a long way on the spanning **tree** . The approach is simpler than DLS and can utilize any non- **tree** link connecting a pair of bridges that have implemented the extended protocol, referred to as Generalized IDLS (GIDLS). GIDLS does not select a non- **tree** link between a pair of GIDLS bridges to be a GIDLS link by comparing the length of the non- **tree** link to that of the corresponding **tree** path. Instead, GIDLS **compares** the " **speed** " of the non- **tree** **link** to that of the corresponding **tree** path. The " **speed** " of the non- **tree** **link** and that of the **tree** path are determined by having one of the GIDLS bridges send to the other GIDLS bridge a special protocol data unit over the non- **tree** link and another over the **tree** path. Separate information has to be kept for every non- **tree** link even though some links will not be used at all. The method of Perlman, et al., cannot guarantee that a forwarding path is no worse than its corresponding **tree** path for any additive metric considered except when the additive metric is delay. Incidentally, this method is backward compatible with the IEEE 802.1 D Spanning **Tree** Bridge Protocol.

Another prior art method dynamically creates a shortest path tree rooted at a...

40/5,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01108601
Method and apparatus for transmitting data over data bus
Verfahren und Vorrichtung zur Ubertragung von Daten uber einen Datenbus
Procede et appareil pour la transmission de donnees sur un bus de donnees
PATENT ASSIGNEE:
SONY CORPORATION, (214021), 7-35 Kitashinagawa 6-chome Shinagawa-ku, Tokyo 141, (JP), (Applicant designated States: all)
INVENTOR:
Kato, Junji, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
Nakano, Takehiko, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Pratt, Richard Wilson et al (46458), D. Young & Co, 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 971508 A2 000112 (Basic)
EP 971508 A3 001108
APPLICATION (CC, No, Date): EP 99303900 990519;
PRIORITY (CC, No, Date): JP 98138033 980520
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H04L-012/40; H04L-012/56; H04L-029/06

ABSTRACT EP 971508 A2
A method and apparatus for transmitting data among devices connected to a serial data bus at maximum speeds are disclosed. Each device may be capable of transmitting data at several speeds. A transmitting device first transmits a data packet to a target recipient device at a maximum transmission speed of the transmitting device. If an acknowledgement signal confirming receipt of the initial data transmission is received from the target recipient, then the transmission speed for subsequent data packet transmissions is set to the speed of the just-transmitted data. Otherwise, the transmission speed is reduced and the process is repeated. Once an acknowledgement is received and the speed is set, the speed may be stored in a memory of the transmitting device for use in future communications with the recipient device. The process is repeated to establish maximum suitable transmission speeds to other target devices connected to the bus. Embodiments of the present invention have particular utility when used in conjunction with an IEEE 1394 serial bus interface in the absence of a bus manager. Following a bus reset operation in which the memory of each device is cleared, individual devices reestablish appropriate data transmission speeds to each of the other devices by transmitting packets at varying speeds, if necessary, until acknowledgements are received.
ABSTRACT WORD COUNT: 214
NOTE:
Figure number on first page: 17

LEGAL STATUS (Type, Pub Date, Kind, Text):

Change:	001108	A2	International Patent Classification changed: 20000915
Application:	20000112	A2	Published application without search report
Examination:	020102	A2	Date of dispatch of the first examination report: 20011115
Examination:	010620	A2	Date of request for examination: 20010419
Search Report:	001108	A3	Separate publication of the search report

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200002	1033
SPEC A	(English)	200002	6957
Total word count - document A			7990
Total word count - document B			0
Total word count - documents A + B			7990

...SPECIFICATION supports the transmission speed of the asynchronous packet. As mentioned earlier, according to the IEEE **1394** standard, if a bus manager is present, it maintains a speed map for the current **topology** of **interconnected** nodes, and supplies the predetermined **speed** information to each of the nodes. In the absence of a bus manager, the predetermined...

```
File 696:DIALOG Telecom. Newsletters 1995-2003/Jun 19
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Set     Items   Description
S1    1558548   TREE OR TREES OR HIERARCH? OR TREEMAP? OR GRID OR GRIDS OR
             TOPOLOG?????? ? OR PYRAMID? ? OR CASCAD? OR SUBTREE? ?
S2    5563897   PARENT? ? OR CHILD OR CHILDREN
S3    3128629   SPEED OR SPEEDS
S4      15544   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (PORT OR PORTS)
S5       7056   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (NODE OR NODES)
S6    3183585   SPEEDIER OR SPEEDIEST OR CELERITY? OR RAPID OR RAPIDLY OR -
             RAPIDER OR RAPIDEST OR RAPIDITY OR RAPIDNESS OR SWIFT???? ?
S7    7561996   FAST OR FASTER OR FASTEST OR FASTNESS OR QUICK???? ?
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S8      305630   (S3 OR S6:S7)(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK???
               ? OR INTERLINK?)
S9        1256   S4:S5(5N)(CONNECT???? ? OR INTERCONNECT? OR LINK??? ? OR I-
               NTERLINK?)
S10    6706882   COMPAR?
S11      97585   S10(5N)(PORT OR PORTS OR NODE OR NODES OR S3 OR S6:S7 OR D-
               EVICE? ? OR BUS OR BUSSES OR BUSES)
S12     311410   S10(5N)(APPARATUS? OR APP?? ? OR NETWORK? ? OR COMPONENT? ?
               OR UNIT OR UNITS OR SYSTEM? ? OR MODULE? ? OR TERMINAL? ? OR
               COMPUTER? ? OR PC OR PCS)
S13      25446   S10(5N)(PCU? ? OR WORKSTATION? OR WORK()STATION? ? OR CPU?
               ? OR CONSOLE? ? OR CLIENT? ? OR MICROPROCESS?R? ? OR MICROCOM-
               PUT?)
S14       8087   S1:S2(S)S11:S13
S15         71   S14(S)S8
S16          4   S14(S)S9
S17         75   S15:S16
S18      27453   1394
S19       2581   (S8 OR S4:S5)(10N)S10
S20          1   S19(S)S18
S21       4609   (S8 OR S4:S5)(20N)S10
S22         12   S21(S)S18
S23         87   S17 OR S22
S24         37   S23/1999:2003
S25         50   S23 NOT S24
S26         34   RD (unique items)
```

26/3,K/31 (Item 2 from file: 674)
DIALOG(R)File 674:Computer News Fulltext

050272
A Switching for all seasons
Special Section: LAN Switching
Choosing the switch that will help fix what ails your net.
Byline: Rolf McClellan
Journal: Network World Page Number: 51
Publication Date: March 04, 1996
Word Count: 2491 Line Count: 237

Text:
... server and/or server throughput are low enough to preclude any significant benefit from higher **speed** server **connections** . Keep in mind that with high-performance servers, a 10M bit/sec server port would functionality. Naturally, these features are reflected in a higher price per **port** as **compared** to fixed-configuration or less expandable switches. Figure 1 provides general guidelines on what characteristics...

... adapters, plus possible disruption of existing applications. A dual-speed LAN switch with a high- **speed** port for **connection** to the backbone increases bandwidth to remote servers more cost effectively because it does not...
... media LANs. A more flexible solution is to deploy another level of switching in a **hierarchy** that allows bandwidth capacity to be scaled up gracefully. In that fashion, you can more...

... growth of workgroup switching, the departmental switch will be increasingly challenged to deliver enough high- **speed** **connections** to keep up with the expanding aggregate bandwidth to the desktop. This means that while...scale up to accommodate larger numbers of shared and dedicated segments, the importance of high- **speed** server **connections** and backbone ports, Layer 3 routing, modular packaging, network management features and fault tolerance increases...

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         (c) 2003 Resp. DB Svcs.
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File 484:Periodical Abs Plustext 1986-2003/Jun W3
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File 553:Wilson Bus. Abs. FullText 1982-2003/May
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File 369:New Scientist 1994-2003/Jun W2
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File 370:Science 1996-1999/Jul W3
         (c) 1999 AAAS
File  20:Dialog Global Reporter 1997-2003/Jun 18
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Set     Items   Description
S1    1557450   TREE OR TREES OR HIERARCH? OR TREEMAP? OR GRID OR GRIDS OR
             TOPOLOG?????? ? OR PYRAMID? ? OR CASCAD? OR SUBTREE? ?
S2    5559435   PARENT? ? OR CHILD OR CHILDREN
S3    3126713   SPEED OR SPEEDS
S4      15534   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (PORT OR PORTS)
S5       7053   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (NODE OR NODES)
S6    3389663   PRIORIT? OR RANK???? ?
S7    1456508   SORT OR SORTS OR SORTED OR SORTING?
S8    9362893   ORGANIS? OR ORGANIZ?
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S9   21554513   PLACE? ? OR PLACING? OR PLACEMENT? OR PLACED OR POSITION???
              ? OR LOCAT???? ? OR LIST OR LISTS OR LISTED OR LISTING? ? OR
             SITUATE? ? OR SITUATING OR SITED
S10    372614   S6:S9(5N)(CONNECT? OR INTERCONNECT? OR LINK??? ? OR INTERL-
             INK?)
S11    468531   S3:S5(S)S6:S9
S12     13631   S11(S)S1:S2
S13       435   S12(S)S10
S14       216   S13/1999:2003
S15       219   S13 NOT S14
S16       173   RD (unique items)
S17     20586   S3:S5(20N)S1
S18       125   S17(S)S10
S19      7463   S11(S)S1
S20       323   S19(S)S10
S21       344   S18 OR S20
S22       137   S21/1999:2003
S23       207   S21 NOT S22
S24       156   RD (unique items)
S25       143   S24 NOT PYRAMID()RESEARCH
S26       134   S25 NOT CASCADE()COMMUNICATIONS
S27       129   S26 NOT (DEREGULAT? OR CASCADIA)
S28       125   S27 NOT CONNECTICUT
S29       121   S28 NOT (ORGANIZER? OR ORGANISER? OR CASCADE()COMMUNICATIO-
             N? OR CASCADING(1W)STYLE?)
S30       120   S29 NOT ORGANISM?
S31       118   S30 NOT BOISE()CASCADE
```

31/3,K/54 (Item 13 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03177720 Supplier Number: 44345214
Cisco to add virtual links to public nets
PC Week, p13
Jan 10, 1994
Language: English Record Type: Abstract
Document Type: Magazine/Journal; Tabloid; General Trade

ABSTRACT:
...feature for its router software called 'virtual interfaces.' Virtual interfaces allow users to create arbitrary **topology** networks. With these networks, each virtual circuit has its own routing protocols, accounting capabilities and...

...between routers. The software allows for better control of the cost of users' public network **connections** by **prioritizing** traffic over various **speed links** , which raise in price as **speeds** go up.
...

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         (c) 2003 ProQuest Info&Learning
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
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Set     Items   Description
S1    1334836   TREE OR TREES OR HIERARCH? OR TREEMAP? OR GRID OR GRIDS OR
            TOPOLOG?????? ? OR PYRAMID? ? OR CASCAD? OR SUBTREE? ?
S2    1675070   PARENT? ? OR CHILD OR CHILDREN
S3    1115132   SPEED OR SPEEDS
S4       1853   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
            (PORT OR PORTS)
S5      15876   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
            (NODE OR NODES)
S6     470604   PRIORIT? OR RANK???? ?
S7     153003   SORT OR SORTS OR SORTED OR SORTING?
S8    2491773   ORGANIS? OR ORGANIZ?
S9    4454333   PLACE? ? OR PLACING? OR PLACEMENT? OR PLACED OR POSITION???
             ? OR LOCAT???? ? OR LIST OR LISTS OR LISTED OR LISTING? ? OR
            SITUATE? ? OR SITUATING OR SITED
S10    160347   S3:S5 AND S6:S9
S11      9505   S10 AND S1:S2
S12     54302   S6:S9(5N)(CONNECT? OR INTERCONNECT? OR LINK??? ? OR INTERL-
            INK?)
S13       316   S11 AND S12
S14     18405   S3:S5(20N)S1:S2
S15        97   S14 AND S12
S16        16   S15/1999:2003
S17        81   S15 NOT S16
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S18 60 RD (unique items)
S19 60 S18 NOT (PYRAMID()RESEARCH OR CASCADE()COMMUNICATION? OR D-EREGULAT? OR CASCADIA OR CONNECTICUT OR ORGANI?ER? OR CASCADI-NG()STYLE? OR ORGANISM? OR BOISE()CASCADE)
S20 57 S19 NOT (WIND()FARM? OR WINDFARM? OR BALL()GRID? ?)
S21 46 S20 NOT (WIND()SPEED? OR PHOTOVOLT? OR TRANSISTOR? OR DIEL-ECT? OR TURBIN? OR LASER? OR TEACHER? OR PASSENGER?)
? t21/7/all

21/7/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6111333 INSPEC Abstract Number: B9901-8375-020, C9901-7410B-119
Title: A distributed intelligent data acquisition system for high voltage substation and test environments
Author(s): Heunis, K.; Vermeulen, H.J.
Author Affiliation: Dept. of Electr. & Electron. Eng., Stellenbosch Univ., South Africa
Conference Title: 33rd Universities Power Engineering Conference. UPEC '98 Conference Proceedings Part vol.1 p.210-13 vol.1
Publisher: Napier Univ, Edinburgh, UK
Publication Date: 1998 Country of Publication: UK 3 vol. (xix+878+20) pp.
ISBN: 0 902703 45 5 Material Identity Number: XX98-01236
Conference Title: Proceedings of 1998 Universities Power Engineering Conference
Conference Date: 8-10 Sept. 1998 Conference Location: Edinburgh, UK
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: This paper describes a data acquisition system topology that has been optimised for use in the high voltage (HV) power system environment. The topology is of a distributed nature in the sense that a digitising probe is implemented close to the kV transducer and the digitised data is transmitted serially via a high-speed optical fibre to an intelligent acquisition unit, also situated in the external substation environment. The acquisition unit accommodates up to four channels and is controlled via an RS485 **link** from a host computer, typically **situated** in the substation. Data acquisition criteria such as sampling **speed**, number of samples, pre-trigger information, etc. can be programmed from the host computer. The **topology** of the acquisition unit allows for real-time digital signal processing such as filtering. The system makes extensive use of field programmable gate array (FPGA) technology to reduce board space and increase programmability, and features a configurable FPGA-based dynamic random access memory (DRAM) module. (4 Refs)
Subfile: B C

21/7/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6091587 INSPEC Abstract Number: B9901-0290T-002, C9901-4185-001
Title: An algorithm for intersecting and trimming parametric meshes
Author(s): Coelho, L.C.G.; Gattass, M.; De Figueiredo, L.H.
Author Affiliation: Dept. of Comput. Sci., PUC, Rio de Janeiro, Brazil
Conference Title: Proceedings SIBGRAPI'98. International Symposium on Computer Graphics, Image Processing, and Vision (Cat. No.98EX237) p. 86-93
Editor(s): da Fontoura Costa, L.; Camara, G.

Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA
Publication Date: 1998 Country of Publication: USA xv+486 pp.
ISBN: 0 8186 9215 4 Material Identity Number: XX98-02927
U.S. Copyright Clearance Center Code: 0 8186 9215 4/98/$10.00
Conference Title: Proceedings SIBGRAPI'98. International Symposium on Computer Graphics, Image Processing, and Vision
Conference Sponsor: Inst. Fisica de Sao Carlos (IFSC-USP); Inst. Pesquisas Espaciais (INPE); Sociedade Brasileira de Computacao (SBC); Fundacao de Amparo a Pesquisa do Estado de Sao Paulo (FAPESP); Fundacao de Amparo a Pesquisa do Estado do Rio de Janeiro (FAPERJ); Sociedade Brasileira de Computacao (SBC); Conselho Nacional de Desenvolvimento Cientifico e Technol. (CNPq); Fundacao Coordenacao de Aperfeioamento de Pessoal de Nivel Superior (CAPES)
Conference Date: 20-23 Oct. 1998 Conference Location: Rio de Janeiro, Brazil
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: We present an algorithm for intersecting finite-element meshes defined on parametric surface patches. The intersection curves are modeled precisely and both meshes are adjusted to the newly formed borders. The algorithm is part of an interactive shell modeling program, which has been used in the design of large offshore oil structures. We avoid unacceptable interaction delays by using a variant of the DCEL data structure that stores **topological** entities in spatial indexing **trees** instead of **linked lists** . These **trees speed** up the intersection computations required to determine points of the trimming curves, and also allows mesh reconstruction using only local queries. (18 Refs)
Subfile: B C

21/7/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5745657 INSPEC Abstract Number: B9712-6250F-116
Title: Locality based location **tracking using virtually hierarchical** link **in personal communications services**
Author(s): SeungJoon Park; DongChun Lee; ChangYong Yang; DaeHun Nyang; JooSeok Song
Author Affiliation: Dept. of Comput. Sci., Yonsei Univ., Seoul, South Korea
Conference Title: 1997 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, PACRIM. 10 Years Networking the Pacific Rim, 1987-1997 (Cat. No.97CH36060) Part vol.1 p.190-3 vol.1
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 2 vol. xxiii+1021 pp.
ISBN: 0 7803 3905 3 Material Identity Number: XX97-02374
U.S. Copyright Clearance Center Code: 0 7803 3905 3/97/$10.00
Conference Title: 1997 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, PACRIM. 10 Years Networking the Pacific Rim, 1987-1997
Conference Date: 20-22 Aug. 1997 Conference Location: Victoria, BC, Canada
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: Personal communications services (PCS) should support several times more users than cellular systems. Using the fact that many call patterns in PCS have the locality between the callers and callees, the proposed mobility management strategy is able to track the user locations

efficiently in a **hierarchically** distributed fashion. In the proposed structure, the larger **number** of **nodes** per **parent** node shows better results. The virtually **hierarchical** link is used for fast call set up, which is useful especially in international roaming. The locality consideration effectively reduces home location register query processings. (11 Refs)
Subfile: B

21/7/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5711249 INSPEC Abstract Number: B9711-6210L-073, C9711-5620-020
Title: On the multidensity gateway location problem for a multilevel high speed internetwork
Author(s): Saha, D.; Mukherjee, A.
Author Affiliation: Dept. of Comput. Sci. & Eng., Jadavpur Univ., Calcutta, India
Journal: Computer Communications vol.20, no.7 p.576-85
Publisher: Elsevier,
Publication Date: 15 Aug. 1997 Country of Publication: UK
CODEN: COCOD7 ISSN: 0140-3664
SICI: 0140-3664(19970815)20:7L.576:MGLP;1-V
Material Identity Number: C213-97011
U.S. Copyright Clearance Center Code: 0140-3664/97/$17.00
Document Number: S0140-3664(97)00016-9
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: This paper addresses the problem of locating the concentrator gateways of different densities in a high **speed** interconnection of networks that are **connected** in a **hierarchical** fashion. The **organization** of gateways can be viewed as an uprooted **tree** , where gateways would be connected to each other in a hierarchy. Gateways at different levels of the tree will have different densities, and the higher the level, the greater the density. Such a multidensity gateway facilitates the sharing of a high speed, high capacity intergateway link among multiple local networks. The objective of this work is to minimize the cost of setting up plus the cost of operating multidensity gateways in an internetwork, subject to some capacity constraint. A mathematical programming model of the problem is developed, and a subgradient heuristic is used to develop a solution procedure for the model. The algorithm is efficient, and produces near optimal solutions always. Extensive simulation studies were conducted to test the performance of the heuristic. Internetworks, consisting of thousands of local networks and hundreds of potential gateway locations, were considered to verify the algorithm. (19 Refs)
Subfile: B C

21/7/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5168488 INSPEC Abstract Number: B9603-6260-064, C9603-7410F-015
Title: Algorithms for optimized node arrangements in ShuffleNet based multihop lightwave networks
Author(s): Banerjee, S.; Mukherjee, B.

Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., Stevens Inst. of Technol., Hoboken, NJ, USA
Journal: Journal of High Speed Networks vol.4, no.4 p.361-83
Publisher: IOS Press,
Publication Date: 1995 Country of Publication: Netherlands
CODEN: JHSNEB ISSN: 0926-6801
SICI: 0926-6801(1995)4:4L.361:AONA;1-U
Material Identity Number: P611-95005
U.S. Copyright Clearance Center Code: 0926-6801/95/$3.50
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: The capabilities of emerging optical technology, viz. dense wavelength division multiplexing (WDM) and tunable optical transmitters and receivers (transceivers) can be exploited to construct lightwave networks. Subsequently, a system can be configured as a broadcast-and-select network in which all of the inputs from various nodes are combined in a star coupler and the mixed optical information is broadcast to all the outputs. Thus, a multitude of virtual network configurations can be superimposed over any given physical network topology. The goal of this study is to exploit the aforementioned capabilities of lightwave technology in order to construct optimized regular multihop networks when the traffic flow among the network nodes is asymmetric. The specific problem addressed here is as follows: given that the network nodes must be connected in a regular **interconnection** pattern and that the node **positions** in the regular network can be adjusted by properly tuning their (optical) transceivers, what is the best node placement in a given regular **topology** ? We have chosen ShuffleNet based regular structure as the model of our network **topology** . ShuffleNet can interconnect a large **number** of **nodes** with a small number of transceivers per node such that information from a source can reach its destination in a small number of hops. However, finding the optimal node placement is a computationally hard problem. So, we formulate efficient heuristic algorithms to design optimized ShuffleNet structures for a given traffic matrix. (24 Refs)
Subfile: B C

21/7/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5130667 INSPEC Abstract Number: B9601-6150P-014, C9601-5620-025
Title: Heuristics for designing telecommunication networks: The p-centralized teleprocessing network design problem
Author(s): Santibanez-Gonzalez, E.; Maculan, N.
Author Affiliation: Inst. of Logic Philos. & Theory of Sci., Niteroi, RJ, Brazil
Conference Title: Telecommunication Systems Conference, Modelling and Analysis p.290-6
Publisher: Vanderbilt Univ, Nahville, TN, USA
Publication Date: 1993 Country of Publication: USA xiii+497 pp.
Conference Title: Proceedings of Telecommunication Systems, Modelling and Analysis Conference
Conference Sponsor: BellSouth Telecommun.; Vanderbilt Univ
Conference Date: 28 Feb.-3 March 1993 Conference Location: Nashville, TN, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: This paper focuses on the p-centralized teleprocessing network design problem. In that problem there are a given set of nodes which receive and send some type of traffic from and to the other nodes.

Considering that network **links** are **placed** between pairs of hubs so that the hubs are fully interconnected, the objective is to select a reduced set of these nodes, so-called hubs, to act as switching points for the traffic in the network. The remaining nodes are connected to one of the hubs. The paper studies a nonlinear (quadratic) 0-1 integer programming formulation for the problem and also presents a linear formulation. We also propose two heuristics to solve it. One of them is based in the solution of the minimum arc-weighted p-clique problem. The other one is based in clustering approach. In this case we use the minimum spanning **tree** problem for clustering the nodes in p groups. Computational results are given for problem sizes up to 42*4 (**number** of **nodes** * **number** of hubs 4). (13 Refs)
Subfile: B C

21/7/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

4991533 INSPEC Abstract Number: B9508-1265B-215, C9508-5120-051
Title: An architecture for intermediate area-time complexity multiplier
Author(s): Islam, F.F.; Tamaru, K.
Author Affiliation: Dept. of Electron., Kyoto Univ., Japan
Conference Title: (Proceedings) 1993 IEEE International Symposium on Circuits and Systems p.1825-8 vol.3
Publisher: IEEE, New York, NY, USA
Publication Date: May 1993 Country of Publication: USA 4 Vols., 2829 pp.
ISBN: 0 7803 1281 3
U.S. Copyright Clearance Center Code: 0-7803-1254-6/93/$03.00
Conference Title: 1993 IEEE International Symposium on Circuits and Systems
Conference Sponsor: IEEE
Conference Date: 3-6 May 1993 Conference Location: Chicago, IL, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The area and time of traditional array and Wallace **tree** multipliers depend on operand bit-size. An intermediate multiplier which has higher **speed** but occupies more area than a traditional array multiplier is proposed. When compared with a traditional Wallace multiplier, it has lower speed and area. The authors' multiplier resembles an array multiplier in terms of regularity in **placement** and **interconnection** of unit computation cells. In contrast to a traditional array multiplier, it computes by introducing multiple computation wave fronts in its partial product core. (4 Refs)
Subfile: B C

21/7/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

4726626 INSPEC Abstract Number: C9409-6160S-024
Title: Spatial joins using seeded trees
Author(s): Ming-Ling Lo; Ravishankar, C.V.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., Michigan Univ., Ann Arbor, MI, USA
Journal: SIGMOD Record vol.23, no.2 p.209-20

Publication Date: June 1994 Country of Publication: USA
CODEN: SRECD8 ISSN: 0163-5808
U.S. Copyright Clearance Center Code: 0163-5808/94/0005$3.50
Conference Title: 1994 ACM SIGMOD International Conference on Management of Data
Conference Sponsor: ACM
Conference Date: 24-27 May 1994 Conference Location: Minneapolis, MN, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P)
Abstract: Existing methods for spatial joins assume the existence of indices for the participating data sets. This assumption is not realistic for applications involving multiple map layer overlays or for queries involving non-spatial selections. We explore a spatial join method that dynamically constructs index **trees** called seeded **trees** at join time. This method uses knowledge of the data sets involved in the join to **speed** up the join process. Seeded **trees** are R- **tree** -like structures, and are divided into the seed levels and the grown levels. The nodes in the seed levels are used to guide tree growth during tree construction. The seed levels can also be used to filter out some input data during construction, thereby reducing **tree** size. We develop a technique that uses intermediate **linked lists** during **tree** construction and significantly **speeds** up the **tree** construction process. The technique allows a large number of random disk accesses during **tree** construction to be replaced by smaller numbers of sequential accesses. Performance studies show that spatial joins using seeded trees outperform those using other methods significantly in terms of disk I/O. The CPU penalties incurred are also lower except when seed-level filtering is used. (16 Refs)
Subfile: C

21/7/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

04208971 INSPEC Abstract Number: B9209-1130B-045, C9209-7410D-130
Title: Timing- and constraint-oriented placement **for** interconnected **LSIs in mainframe design**
Author(s): Ogawa, Y.; Itoh, T.; Miki, Y.; Ishii, T.; Sato, Y.; Toyoshima, R.
Author Affiliation: Hitachi Ltd., Tokyo, Japan
Conference Title: 28th ACM/IEEE Design Automation Conference. Proceedings 1991 (ACM Order No. 477910 & IEEE Cat. No.91CH3014-8) p.253-8
Publisher: ACM, New York, NY, USA
Publication Date: 1991 Country of Publication: USA xxiii+783 pp.
ISBN: 0 89791 395 7
U.S. Copyright Clearance Center Code: 0 89791 395 7/91/0006-0253$1.50
Conference Sponsor: ACM; IEEE
Conference Date: 17-21 June 1991 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: Timing- and constraint-oriented placement procedures are proposed to reduce design time and cost. These goals are (1) optimizing the intra and inter LSI delays, (2) observance of several electrical constraints such as simultaneous switching, and (3) high-precision and high- **speed** delay calculation. **Hierarchical** pin assignment, timing-driven placement, and high- **speed** and precision timing analysis are proposed for achieving the above goals. Such algorithms are applied to a

physical **hierarchy** containing 12 thousand gate ECL gate-array LSIs for the Hitachi M-880, a high-end mainframe computer. Using such algorithms, the physical design is greatly improved by optimizing timing and guaranteeing high wirability, i.e., by reducing the errors and time of error corrections. (17 Refs)
Subfile: B C

21/7/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

04143898 INSPEC Abstract Number: C9206-5290-032
Title: An efficient static topology for modeling ASOCS
Author(s): Rudolph, G.L.; Martinez, T.R.
Author Affiliation: Dept. of Comput. Sci., Brigham Young Univ., Provo, UT, USA
Conference Title: Artificial Neural Networks. Proceedings of the 1991 International Conference. ICANN-91 p.729-34 vol.1
Editor(s): Kohonen, T.; Makisara, K.; Simula, O.; Kangas, J.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1991 Country of Publication: Netherlands 2 vol. xix+1819 pp.
ISBN: 0 444 89178 1
Conference Date: 24-28 June 1991 Conference Location: Espoo, Finland
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: ASOCS (adaptive self-organizing concurrent systems) are a class of **connectionist** computational models which feature self- **organized** learning and parallel execution. One area of ASOCS research is the development of an efficient implementation of ASOCS using current technology. A result of this research is the Location-Independent ASOCS model (LIA). LIA uses a parallel, asynchronous network of independent nodes, which leads to an efficient physical realization using current technology. The paper reviews the behaviour of the LIA model, and shows how a static binary tree topology efficiently supports that behavior. The binary **tree topology** allows for O(log(n)) learning and execution times, where n is the **number** of **nodes** in the network. (9 Refs)
Subfile: C

21/7/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

04047867 INSPEC Abstract Number: B9201-6150M-034, C9201-5640-035
Title: Product forms for random access schemes
Author(s): van Dijk, N.M.
Author Affiliation: Free Univ., Fac. of Econ. & Econometries, Amsterdam, Netherlands
Journal: Computer Networks and ISDN Systems vol.22, no.4 p.303-17
Publication Date: 14 Oct. 1991 Country of Publication: Netherlands
CODEN: CNISE9 ISSN: 0169-7552
U.S. Copyright Clearance Center Code: 0169-7552/91/03.50
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: A unifying framework is presented to conclude explicit product form expressions for the steady state distribution of busy sources (transmitters, lines) for random access communication protocols. Transmission times and packet lengths are generally distributed. The main results are: an insensitive product form expression; a concrete condition

in terms of system protocols; and a generalization of product form random access protocols. These results unify and extend known results. Particularly it includes CSMA protocols with non-exponential transmissions and packets, state dependent transmission **speeds** , and link selective characteristics. A variety of 'novel' examples is given such as with **hierarchical** circuit switching, synchronous serving, randomized grading, message **priorities** , error probabilities, **link** selective transmissions and an extension of rude CSMA. (40 Refs)
Subfile: B C

21/7/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

03872853 INSPEC Abstract Number: B91034045
Title: Switching integrated broadband services by sort-banyan networks
Author(s): Hui, J.
Author Affiliation: Dept. of Electr. & Comput. Eng., Rutgers Univ., Piscataway, NJ, USA
Journal: Proceedings of the IEEE vol.79, no.2 p.145-54
Publication Date: Feb. 1991 Country of Publication: USA
CODEN: IEEPAD ISSN: 0018-9219
U.S. Copyright Clearance Center Code: 0018-9219/91/0200-0145$01.00
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P)
Abstract: Substantial attention has recently been given to the implementation of sort-banyan networks for switching asynchronous transfer mode (ATM) transmission links in a BISDN (broadband integrated service digital network) network. The author gives a three-dimensional view of the theory and implementation of switching, as well as variations of the basic scheme. ATM switches are classified as blocking versus nonblocking, unicast versus multicast, and input queued versus output queued. Sorting networks structured by a three-dimensional **interconnection** topology are studied. A **sorting** network, when coupled with a banyan routing network structured in three dimensions, becomes a self-routing and nonblocking switching network. This three-dimensional **topology** allows CMOS VLSI implementations of the subnetworks and interconnection of these subnetworks at a **speed** of 150 Mb/s and beyond. The sorting mechanism can also be used for output conflict resolution, subsequently making the switch suitable for ATM switching. Recent enhancements, which provide features such as parallelism, trunk grouping, and modularity, are also described. These features enhance the throughput/delay performance, provide better fault and synchronization tolerance, and enable more economical growth for switch size. (18 Refs)
Subfile: B

21/7/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

03684610 INSPEC Abstract Number: B90051464, C90052156
Title: Corporate communication system by LAN interconnection
Author(s): Danthine, A.; Hauzeur, B.; Henquet, P.; Constantinidis, C.; Fagnoule, D.; Cornette, V.
Author Affiliation: Inst. d'Electr., Leige Univ., Belgium
Conference Title: Information Technology for Organisational Systems. Concepts for Increased Competitiveness. Proceedings of the First European Conference - EURINFO '88 p.315-26
Editor(s): Bullinger, H.J.; Protonotarios, E.N.; Bouwhuis, D.; Reim, F.

Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1988 Country of Publication: Netherlands xxxi+1187 pp.
ISBN: 0 444 70427 2
Conference Date: 16-20 May 1988 Conference Location: Athens, Greece
Language: English Document Type: Conference Paper (PA)
Treatment: Bibliography (B); Practical (P)
Abstract: A corporate communication system will be based on a **hierarchy** of LANs where a high **speed** backbone network will play an essential role, especially on a broad site. The basic characteristics of the BWN (backbone wideband network) in ESPRIT project 73 are presented (fiber optic with data rate of 134 Mbps on a ring topology with a token bus without **priority**). The **interconnection** of the heterogeneous LANs relies not only on the backbone network but also on the high performance gateways. The interface to the public domain is based on a gateway giving access to the wideband public services and an experiment of video conferencing at 2 Mbps will demonstrate the multi-media capability of the BWN. Following a short presentation of the system assessment methodology, the first measured results are discussed. They are related to the throughput of the interface to the MAC and to the performance of the internet gateways. The network management problem is also briefly discussed. (56 Refs)
Subfile: B C

21/7/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

03619217 INSPEC Abstract Number: A90066169, C90032636
Title: New computerized control system for the Rossendorf Research Reactor
Author(s): Klebau, J.; Lindner, A.; Ziegenbein, D.
Author Affiliation: Akad. der Wissenschaften, Zentralinst. fur Kernforschung Rossendorf, East Germany
Journal: Kernenergie vol.32, no.12 p.466-9
Publication Date: Dec. 1989 Country of Publication: East Germany
CODEN: KERNAQ ISSN: 0023-0642
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The Rossendorf Research Reactor (RRR) with a thermal output of 10 MW was put into operation 30 years ago. Now the reactor is under reconstruction. The main reactor components are renewed and the control and instrumentation system is backfitted by a new computerized control system. The hardware of the new system consists of GDR-produced components. The system has a **hierarchical** structure. Various basic units which are **situated** nearby the technological process are **linked** with two main computers via a high **speed** serial bus. The control system has to deal with the following problems: (1) acquisition, surveillance and storage of data; (2) optimal reactor shut-down regarding to the minimization of xenon poisoning; (3) radiation protection of the reactor building; (4) on-line disturbance analysis; and (5) man-machine communication. The experience gained by various methods of man-machine communication and some conclusions regarding the further development of the system are discussed. The new control system at the RRR may be seen as a prototype system for design and development of computerized operator support systems for the nuclear power plants in the GDR. (8 Refs)
Subfile: A C

21/7/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

03158965 INSPEC Abstract Number: C88039758
Title: Interconnection networks in multiprocessor computers: a review
Author(s): Stepanyan, S.O.
Journal: Avtomatika i Vychislitel'naya Tekhnika vol.21, no.3 p. 31-43
Publication Date: 1987 Country of Publication: USSR
CODEN: AVYTAK ISSN: 0132-4160
Translated in: Automatic Control and Computer Sciences vol.21, no.3 p.26-36
Publication Date: 1987 Country of Publication: USA
CODEN: ACCSCE ISSN: 0146-4116
U.S. Copyright Clearance Center Code: 0146-4116/87/$20.00
Language: English Document Type: Journal Paper (JP)
Treatment: Bibliography (B); Practical (P)
Abstract: A classification and a brief description of the architecture of multiprocessor computers are presented, emphasizing the role of **interconnection** networks in the **organization** of parallel and distributed computations. The **topological** structures of static and dynamic interconnection networks are reviewed. Special aspects of **speed** , fault tolerance, combinatoric capabilities, control **organization** , and hardware implementation of **interconnection** networks are discussed. (106 Refs)
Subfile: C

21/7/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

02988079 INSPEC Abstract Number: B87059620, C87059319
Title: A pipeline sorting chip
Author(s): Tsuda, N.; Satoh, T.; Kawada, T.
Author Affiliation: NTT, Tokyo, Japan
Conference Title: 1987 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC. First Edition p.270-1, 422
Publisher: Lewis Winner, Coral Gables, FL, USA
Publication Date: Feb. 1987 Country of Publication: USA 518 pp.
U.S. Copyright Clearance Center Code: 0193-6530/87/0000-0270$01.00
Conference Sponsor: IEEE; Univ. Pennsylvania
Conference Date: 25-27 Feb. 1987 Conference Location: New York, NY, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Summary form only given. A compact hardware sorter that can handle many records in linear time is necessary for high- **speed** database retrieval. The design of a pipeline sorting chip with a linear array structure as well as **hierarchical** redundancy techniques, making a larger chip feasible, is described. The chip uses a pipelined insertion sorting algorithm, and can be used as a high-speed one-chip sorter that is at least 20 times faster than an ordinary software sorting process. Moreover, it can also be applied to a multiway merger for mass-record sorting. The basic structure of the chip is a cascode- **connected** 40-element **sorting** array. Each **sorting** element has a 1-b width comparator and two 16-b RAMs. The sorting operation can be done while the records are repeatedly input and then output in a 1-b-wide data stream from one side of the I/O port of the array. In this operation, each sorting element executes synchronized comparison-transferral actions in a successive pipelined manner. The chip

has a total RAM capacity of 80*16-b and 3-Mb/s I/O throughput. This means that 80 16-b records can be sorted in about 800 ms through a single continuous input-output operation. (2 Refs)
Subfile: B C

21/7/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

02967429 INSPEC Abstract Number: C87051095
Title: A dynamic programming approach to the optimal design of tree-like networks
Author(s): Walters, G.A.
Author Affiliation: Dept. of Eng. Sci., Exeter Univ., UK
Conference Title: Proceedings of the International Conference on Optimization: Techniques and Applications - ICOTA p.487-96
Editor(s): Teo, K.L.; Paul, H.; Chew, K.L.; Wang, C.M.
Publisher: Nat. Univ. Singapore, Singapore
Publication Date: 1987 Country of Publication: Singapore 1153 pp.
Conference Date: 8-10 April 1987 Conference Location: Singapore
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: Many networks in engineering are designed as trees. Typical examples are systems for sewerage, irrigation, gas collection and distribution. The author has developed methods of using dynamic programming to generate the network with the least construction cost for two classes of problem. The first class of problem is that in which certain nodes in a network have freedom in the **positions** they can adopt, whilst the **connectivity** of the network remains fixed. The second class of problem is that of determining the optimum way of connecting up a large **number** of **nodes** , some or all of which are sources (or sinks) of flow, to form a **tree** network, where nodes are now considered fixed in location. In this problem the flow along each arc is initially unknown as the connectivity of the network is not predetermined. The methods are described in detail, with examples of their application to realistic design situations. (15 Refs)
Subfile: C

21/7/18 (Item 18 from file: 2)
DIALOG(R)File 2:INSPEC

02774741 INSPEC Abstract Number: B86066960, C86057477
Title: Structured custom integrated circuit design methodology
Author(s): Westbrook, G.
Author Affiliation: GE Calma Co., Milpitas, CA, USA
Conference Title: Automated Design and Engineering for Electronics West. Proceedings of the Technical Sessions p.202-4
Publisher: Cahners Exposition Group, Des Plaines, IL, USA
Publication Date: 1986 Country of Publication: USA 304 pp.
Conference Date: 11-13 March 1986 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Structured custom is an IC design automation methodology that combines the hand craft flexibility of the full custom design approach with the **speed** and automation of semicustom design. The structured custom method impacts cell design, cell design migration, and **hierarchical** cell **placement** and **interconnect** routing. The application specific integrated

circuit (ASIC) market today offers a prelude to the need for a structured custom approach. Applications for ASICs penetrate all industry segments, design groups pursuing multiple chip types, and multiple systems. (0 Refs)
Subfile: B C

21/7/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC

02645673 INSPEC Abstract Number: C86023689
Title: Multicluster: an MIMD system for computer vision
Author(s): Reeves, A.P.
Author Affiliation: Sch. of Electr. Eng., Cornell Univ., Ithaca, NY, USA
Conference Title: Integrated Technology for Parallel Image Processing p.39-56
Editor(s): Levialdi, S.
Publisher: Academic Press, London, UK
Publication Date: 1985 Country of Publication: UK x+236 pp.
ISBN: 0 12 444820 8
Conference Date: June 1983 Conference Location: Polignano, Italy
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Multicluster is a general MIMD framework for high-speed parallel computation. A system in this framework consists of a set of computational modules called clusters; each cluster contains one or more 32-bit microprocessors, high- **speed** arithmetic support, local memory and an intercluster interface. The processor interconnection scheme will involve a **hierarchy** of at least two levels the intracluster network, which will be determined by technological considerations and the intercluster network, which will be based more on algorithmic and general architecture considerations. The system should be tolerant to the failure of one or more clusters (or intercluster connections) and should suffer a graceful degradation of performance as clusters of parts of clusters fail. Furthermore, it should be possible to add new processors to a system as the demands on the system increase. This chapter is divided into three main sections. First, the Multicluster hardware framework is described. A major hardware design problem, the **organisation** of the global **interconnection** network, is outlined. Second, software techniques for implementing algorithms on the Multicluster framework are considered. Finally, a simple near-neighbor primitive algorithm is analysed to determine global network design parameters. (11 Refs)
Subfile: C

21/7/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC

02423458 INSPEC Abstract Number: C85019849
Title: Sorting algorithms in an event-oriented simulation of a computer network
Author(s): Fritz, J.V.; Wahrenberger, D.E.
Author Affiliation: Div. of Space Syst., Naval Res. Lab., Washington, DC, USA
Conference Title: Modeling and Simulation. Vol.14. Proceedings of the Fourteenth Annual Pittsburgh Conference p.265-70
Editor(s): Vogt, W.G.; Mickle, M.H.
Publisher: ISA, Research Triangle Park, NC, USA
Publication Date: 1983 Country of Publication: USA 3 vol. 1457 pp.
Conference Sponsor: Univ. Pittsburgh; IEEE; ISA; SCS; Int. Assoc. Math. &

Comput. Simulation
Conference Date: 21-22 April 1983 Conference Location: Pittsburgh, PA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: Some sorting algorithms are considered for use in an event-oriented simulation of a completely connected computer network. In particular, a scheme for **hierarchical** sorting of the event list is considered for the purpose of increasing the **speed** of the simulation. (8 Refs)
Subfile: C

21/7/21 (Item 21 from file: 2)
DIALOG(R)File 2:INSPEC

01271063 INSPEC Abstract Number: C78029293
Title: The efficiency of two indexed priority queue algorithms
Author(s): Nevalainen, O.; Teuhola, J.
Author Affiliation: Dept. of Computer Sci., Univ. of Turku, Turku, Finland
Journal: BIT (Nordisk Tidskrift for Informationsbehandling) vol.18, no.3 p.320-33
Publication Date: 1978 Country of Publication: Sweden
CODEN: NBITAB ISSN: 0006-3835
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: Two **priority** queue algorithms, a **linked** linear sublist, and a p- **subtree** algorithm, are analysed. Both of them use a search index that **speeds** up finding the correct sublist/ **subtree** . In most cases the methods require a short processing time for the so-called HOLD-operation of the discrete event simulation. The relative power of the algorithms depends on the ratio r of the total number of elements in the queue and the size of the search index. For large values of r(>or=16) the p-subtree algorithm is to be preferred. However, the more primitive data structure used by the sublist algorithm makes it possible to use a larger index leading to a smaller ratio r. (13 Refs)
Subfile: C

21/7/22 (Item 22 from file: 2)
DIALOG(R)File 2:INSPEC

00948943 INSPEC Abstract Number: C76021751
Title: A list insertion sort for keys with arbitrary key distribution
Author(s): Janko, W.
Author Affiliation: Hochschule fur Welthandel, Wien, Austria
Journal: ACM Transactions on Mathematical Software vol.2, no.2 p. 143-53
Publication Date: June 1976 Country of Publication: USA
CODEN: ACMSCU ISSN: 0098-3500
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Theoretical (T)
Abstract: An algorithm is described which is an insertion **sort** producing a single **linked list** . The **sorting** method is insensitive to the key distribution. In comparison with alternative insertion sort algorithms like Shellsort algorithms, simple list insertion, and binary **tree** insertion, this subroutine is comparable in **speed** with sorting

algorithms of the Shellsort type. The number of comparisons is determined by the term O(n/sup 1.5/). In comparison with known alternative sorting methods like quicksort and two-way merge, timing experiments with integer keys showed that the application of the algorithm is very favorable for 5<or approximately=n<or approximately=50. This may change for extremely long keys and for an ascending or a descending trend in the keys. In the first case, an algorithm which minimizes the number of comparisons (like two-way list merge) is usually faster for sufficiently large n; in the second case, the given algorithm can be favorable even for very large values of n. (6 Refs)
Subfile: C

21/7/23 (Item 23 from file: 2)
DIALOG(R)File 2:INSPEC

00273403 INSPEC Abstract Number: B71023209
Title: Synchronizing and multiplexing in a digital transmission hierarchy
Author(s): Pan, J.W.
Author Affiliation: Bell Telephone Labs., Holmdel, NJ, USA
Conference Title: 1971 IEEE International Convention Digest p.176-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1971 Country of Publication: USA 643 pp.
Conference Sponsor: IEEE
Conference Date: 22-25 March 1971 Conference Location: New York, NY, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A digital transmission facility can be made up of a digital transmission line with regenerative repeaters or it can be derived from an analog facility by appropriate conversion at the terminals. A digital facility operating at a lower rate can also be derived from a part of a higher **speed** facility by multiplexing. This paper discusses the **hierarchy** of digital transmission systems either in service or in development in the Bell System and the **organization** of the digital multiplexers that **interconnect** facilities of various rates.
Subfile: B

21/7/24 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

0139958 NTIS Accession Number: AD-664 059/XAB
Diagonal Display - a New Technique for Graphic Representation of Complex Topological Networks
(Final rept)
Garfield, E. ; Sher, I. H.
Institute for Scientific Information Inc Philadelphia Pa
Corp. Source Codes: 180250
Report No.: AFOSR-68-0115
Sep 67 92p
Journal Announcement: USGRDR6805
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A05/MF A01
Contract No.: AF 49(638)-1547; AF-9769; 976901

A new method has been developed for automatically drawing diagrams of **topological** networks containing a large **number** of interconnected **nodes** representing interrelated items, concepts, or events. The method allows a display of at least 100 nodes, permits an unlimited number of interconnections among nodes, is algorithmically manipulable, and is felt to be simple and aesthetically pleasing. Many known techniques for automatically drawing networks or graphs were reviewed, including those used in computer flow charting, electric circuit drawing, logical analysis, etc. A series of formats for displaying topological networks was tried, including a new format called 'Diagonal Display'. This involves drawing nodes in a diagonal array and showing interconnections by rectangular lines in the adjacent areas. The upper or lower elbows of the lines for **connecting** edges fall into **positions** which correspond to the coordinates of a matrix representation of the network. To implement the automatic display by a computer-activated pen plotter, a program was written for a system employing an IBM 1401 computer and a Calcomp 563 plotter. The original impetus for this study was the need to display networks of bibliographic citations used in historical research or in searching scientific and technical literature. Other applications are also considered, including PERT diagrams, organizational charts, etc.

21/7/25 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04871506 E.I. No: EIP97113930254
Title: Locality based location **tracking using virtually hierarchical** link **in personal communications services**
Author: Park, SeungJoon; Lee, DongChun; Yang, ChangYong; Nyang, DaeHun; Song, JooSeok
Corporate Source: Yonsei Univ, Seoul, South Korea
Conference Title: Proceedings of the 1997 6th IEEE Pacific Rim Conference on Communications, Computers and Signal Processing. Part 1 (of 2)
Conference Location: Victoria, Can Conference Date: 19970820-19970822
Sponsor: IEEE
E.I. Conference No.: 47264
Source: IEEE Pacific RIM Conference on Communications, Computers, and Signal Processing - Proceedings v 1 1997. IEEE, Piscataway, NJ, USA,97CH36060. p 190-193
Publication Year: 1997
CODEN: 002121
Language: English
Document Type: CA; (Conference Article) Treatment: G; (General Review)
Journal Announcement: 9801W2
Abstract: Personal communications services (PCS) should support a number of users that is several times larger than that of cellular systems. Using the fact that many call patterns in PCS have the locality between the callers and callees, the proposed mobility management strategy is able to track the user locations efficiently in a **hierarchically** distributed fashion. In the proposed structure, the larger **number** of **nodes** per **parent** node shows better results. The virtually **hierarchical** link is used for fast call set up, which is useful especially in the international roaming. The locality consideration effectively reduces the HLR query processings compared to otherwise. (Author abstract) 11 Refs.

21/7/26 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04820324 E.I. No: EIP97093822947
Title: Multicasting solution for ATM video applications
Author: Tsai, Jer-Min; Fang, Hsin-Hsiung; Ju, Chi-Cheng; Lee, Chen-Yi
Corporate Source: Natl Chiao Tung Univ, Hsinchu, Taiwan
Conference Title: Proceedings of the 1997 IEEE International Symposium on Circuits and Systems, ISCAS'97. Part 4 (of 4)
Conference Location: Hong Kong, Hong Kong Conference Date: 19970609-19970612
Sponsor: IEEE
E.I. Conference No.: 46961
Source: Digital Signal Processing Industrial Applications Proceedings - IEEE International Symposium on Circuits and Systems v 4 1997. IEEE, Piscataway, NJ, USA,97CB35987. p 2781-2784
Publication Year: 1997
CODEN: PICSDI ISSN: 0271-4310
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications)
Journal Announcement: 9711W1
Abstract: This paper presents a multicasting solution for shared-buffer ATM switch. The cell duplicating function is performed by a one-to-many modified demux circuit. A shared multicast server is used to translate input multicast cells to find destination ports and corresponding routing information. By using **link - list** based ring structure, the multicast server can provide high **speed** (5ns for search entry in 256-entry block in 0.8 mu m CMOS process) and **cascadable** multicast translating function. In addition, the channel complexity of multipoint-to-multipoint multicast applications can be reduced to N channels per N users. The shared-buffer controller is modified by adding controlling and scheduling functions for multicasting queues to process the multicast feature. (Author abstract) 10 Refs.

21/7/27 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04575893 E.I. No: EIP96123472354
Title: Design and analysis of a serial link interconnection network architecture
Author: Sharif, Hamid R.; Vakilzadian, Hamid; Nagisetty, Sreekanth
Corporate Source: Univ of Nebraska-Lincoln, Omaha, NE, USA
Source: Computer Systems Science and Engineering v 11 n 5 Sep 1996. p 287-299
Publication Year: 1996
CODEN: CSSEEI ISSN: 0267-6192
Language: English
Document Type: JA; (Journal Article) Treatment: G; (General Review)
Journal Announcement: 9702W1
Abstract: We present a study of an experimental interconnection network in this paper. This architecture is based on ultra-high speed full-duplex serial links and columns of switches. The **interconnection** network **places** the outer columns of the switches in a connected binary tree topology while the innermost columns are linked point-to-point. Switches provide routing through the interconnection network. We have discussed the characteristics of SLIN in terms of organization, system design, performance measures, cost-effectiveness and load-balancing potential. Analytical and computer models of the SLIN architecture are designed to provide system performance measures. These measures are compared with other related interconnection network architectures. The results of the SLIN models suggest a promising cost/performance ratio, a far better link

utilization, and inherently suitable for load balancing. (Author abstract) 19 Refs.

21/7/28 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03953250 E.I. No: EIP94101422831
Title: Spatial joins using seeded trees
Author: Lo, Ming-Ling; Ravishankar, Chinya V.
Corporate Source: Univ of Michigan-Ann Arbor, Ann Arbor, MI, USA
Conference Title: Proceedings of the 1994 ACM SIGMOD International Conference on Management of Data
Conference Location: Minneapolis, MN, USA Conference Date: 19940524-19940527
Sponsor: SIGMOD
E.I. Conference No.: 20693
Source: Proceedings of the ACM SIGMOD International Conference on Management of Data v 23 n 2 Jun 1994. Publ by ACM, New York, NY, USA. p 209-220
Publication Year: 1994
CODEN: 000462 ISBN: 0-89791-639-5
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical); A; (Applications)
Journal Announcement: 9411W3
Abstract: In this paper, we explore a spatial join method that dynamically constructs index **trees** called seeded **trees** at join time. This method uses knowledge of the data sets involved in the join to **speed** up the join process. Seeded **trees** are R- **tree** -like structures, and are divided into the seed levels and the grown levels. The nodes in the seed levels are used to guide tree growth during tree construction. The seed levels can also be used to filter out some input data during construction, thereby reducing **tree** size. We develop a technique that uses intermediate **linked lists** during **tree** construction and significantly **speeds** up the **tree** construction process. The technique allows a large number of random disk accesses during **tree** construction to be replaced by smaller numbers of sequential accesses. Our performance studies show that spatial joins using seeded trees outperform those using other methods significantly in terms of disk I/O. The CPU penalties incurred are also lower except when seed-level filtering is used. (Edited author abstract) Refs.

21/7/29 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02877262 E.I. Monthly No: EIM9003-012804
Title: Function of a connection network between host and processing elements in massively parallel computer systems.
Author: Bridges, Timothy
Corporate Source: Indiana Univ, Comput Sci Dep, Bloomington, IN, USA
Conference Title: Proceedings: The 2nd Symposium on the Frontiers of Massively Parallel Computations
Conference Location: Fairfax, VA, USA Conference Date: 19881010
E.I. Conference No.: 12769
Source: Proc 2nd Symp Front Massively Parallel Comput. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. Available from IEEE Service Cent (cat n 88CH2649-2), Piscataway, NJ, USA. p 455-458

Publication Year: 1988
Language: English
Document Type: PA; (Conference Paper) Treatment: T; (Theoretical); A; (Applications)
Journal Announcement: 9003
Abstract: The authors examine the function of a connection network between massive numbers of processing elements (PEs) and a single host by comparing the data structure machine (DSM), whose major connection network is a computationally powerful binary tree with the host connected at the root, and the Connection Machine (CM), which provides a very rich and general PE-to-PE connection network, but whose connection to the host is little more than a buffered wire. The binary **tree** network used in the DSM can be utilized to achieve asymptotic improvements in **speed** for algorithms that maintain, locate, and utilize data parallelism in data structures that can be characterized by a high degree of locality. For example, SUM, MAX, LEFTMOST, and INDEX are all constant time operations on DSM lists, while corresponding CM algorithms can require linear time simply to find and mark **lists** . The linear **connection** topology of the DSM's processing elements is able to outperform the binary n-cube topology of the CM processing elements by utilizing an additional connection network to the host. In this case a binary tree network is able to maintain and exploit locality properties within data structures stored in the array of processing elements at the leaf level. 7 Refs.

21/7/30 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02800504 E.I. Monthly No: EI8910099305
Title: Design of highly reliable tree architectures.
Author: Srinivasan, K. Y.; Sood, A. K.
Corporate Source: Univ of Toledo, Toledo, OH, USA
Source: Computers & Electrical Engineering v 14 n 1-2 1988 p 43-52
Publication Year: 1988
CODEN: CPEEBQ ISSN: 0045-7906
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 8910
Abstract: It is established that tree interconnections provide the most natural **interconnect** architecture for **hierarchically organized** distributed computing systems. One advantage of the **tree** architecture is the O(log N) **speed** of information exchange between any two nodes of an N node system. Another advantage is that the **tree** architecture can naturally map several important classes of problems that can be described as divide-and-conquer algorithms. We address the issue of fault-tolerance in binary tree architectures and present two new reliable tree architectures: the L-tree and the LN-tree. The L-tree is formed by augmenting the simplex binary tree with redundant links, the LN-tree is formed by augmenting the simplex binary tree with redundant nodes as well as links. Comparing the fault-tolerance performance of these two tree structures with other augmented tree structures previously proposed, we find that the L-tree reliable than existing fault-tolerant tree structures and has the further advantage of permitting simple algorithmic routing. The L-tree tolerates faults with a degradation in performance, however, whereas the LN-tree is not only highly reliable, but also maintains a rigid tree structure in the event of faults. (Edited author abstract) 14 Refs.

21/7/31 (Item 7 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

02644361 E.I. Monthly No: EIM8809-048229
Title: OPTIMAL FACILITY SELECTION ALGORITHM FOR A SYNCHRONIZATION NETWORK.
Author: Li, Kwang-Fu
Corporate Source: Bell Communications Research, Red Bank, NJ, USA
Conference Title: IEEE/IEICE Global Telecommunications Conference 1987 - Conference Record.
Conference Location: Tokyo, Jpn Conference Date: 19871115
Sponsor: IEEE, Communications Soc, New York, NY, USA; Inst of Electronics, Information and Communication Engineers of Japan, Tokyo, Jpn; Foundation for Advancement of Int Science
E.I. Conference No.: 11418
Source: Publ by Ohmsha Ltd, Tokyo, Jpn. Available from IEEE Service Cent (Cat n 87CH2520-5), Piscataway, NJ, USA p 1043-1047
Publication Year: 1987
ISBN: 4-274-03188-8
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8809
Abstract: A mathematical model is introduced for selecting the most available primary and secondary synchronization reference links between digital offices that aids in meeting synchronization network design requirements. The crucial part of this model is the paired comparison among the factors that characterize all the available facility candidates: history record, activity, facility length, cable type, protection switching, facility type, number of multiplexers, number of offices served, existing synchronization links in route, and **number** of **cascaded nodes** . A set of numerical weights form a judgement matrix which interprets the interrelationships among factors. From the given judgement matrix a vector of priorities, in mathematical terms the principal eigenvector, is computed. Computing the maximal eigenvalue estimates the consistency of the judgement matrix. 2 refs.

21/7/32 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01896306 E.I. Monthly No: EIM8510-058474
Title: HIGH SPEED FIBER OPTIC NETWORKING.
Author: Husain, A.; Warrior, J.; Franta, William R.
Corporate Source: Honeywell Control Systems, Technology Strategy Cent, Roseville, MN, USA
Conference Title: Proceedings - FOC/LAN 83, Papers presented at the Seventh International Fiber Optic Communications and Local Area Networks Exposition.
Conference Location: Atlantic City, NJ, USA Conference Date: 19831010
Sponsor: Information Gatekeepers Inc, Boston, MA, USA
E.I. Conference No.: 06801
Source: Publ by Information Gatekeepers Inc, Boston, MA, USA p 216-221
Publication Year: 1983
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8510
Abstract: The impact of utilizing very-high-speed fiber optic channels (> 50 Mbps) on local area networking (LAN) architecture is discussed. The effects of exploiting high speed on each of the levels of the International Standards **Organization** (ISO) Open Systems **Interconnect** (OSI) model are

presented. The advantages and constraints placed on high- **speed** networking by using the fiber optic media are discussed. Recommendations on the preferred **topology** and access protocol classes most applicable to high-**speed** fiber optic LANs are made. 12 refs.

21/7/33 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01461925 E.I. Monthly No: EIM8312-088887
Title: HARDWARE CONSIDERATIONS IN LOCAL AREA NETWORKS.
Author: Iyer, Venkatraman; Joshi, Sunil P.
Corporate Source: Advanced Micro Devices Inc, Sunnyvale, Calif, USA
Conference Title: Conference Record - Midcon/82.
Conference Location: Dallas, Tex, USA Conference Date: 19821130
E.I. Conference No.: 02794
Source: Conference Record - Midcon 1982. Publ by Electronic Conventions Inc, El Segundo, Calif, USA. Distributed by Western Periodicals Co, North Hollywood, Calif, USA 20. 2, 11p
Publication Year: 1982
CODEN: MCORDY
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8312

21/7/34 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00372680 E.I. Monthly No: EI7406036754
Title: Hydraulic Screw Down and Gage Control in Cold Rolling Mills.
Title: HYDRAULISCHE WALZENANSTELLUNG UND BANDDICKENREGELUNG IN KALTWALZWERKEN.
Author: Schoenert, Dieter; Thome, Heinz Josef
Source: Stahl und Eisen v 94 n 5 Feb 28 1974 p 175-182
Publication Year: 1974
CODEN: STEIA3 ISSN: 0340-479X
Language: GERMAN
Journal Announcement: 7406
Abstract: An analysis is presented of the interrelations in a coupled process system, using a cold rolling reversing mill as an example. Discussed are the structures of process systems with couplings, the structure of the control system of a hydraulic screw down, methods for increasing the inherent damping of the system, hydraulic **position** control in **cascade connection** , the high **speed** roll gap opening, strip gage control with short time constant, and gage statistics. In German.

21/7/35 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06209872 Genuine Article#: YC082 Number of References: 75
Title: Passivity-based control of a class of Blondel-Park transformable electric machines
Author(s): Nicklasson PJ (REPRINT) ; Ortega R; EspinosaPerez G
Corporate Source: SINTEF,ELECT & CYBERNET AUTOMAT CONTROL/N-7034 TRONDHEIM//NORWAY/ (REPRINT); ECOLE SUPER ELECT,SIGNAUX & SYST LAB,

CNRS/F-91192 GIF SUR YVETTE//FRANCE/; UNIV NACL AUTONOMA MEXICO,INST ING/MEXICO CITY 04510/DF/MEXICO/
Journal: MODELING IDENTIFICATION AND CONTROL, 1997, V18, N4 (OCT), P273-305
ISSN: 0332-7353 Publication date: 19971000
Publisher: MIC, DIV ENG CYBERNETICS, 7034 TRONDHEIM, NORWAY
Language: English Document Type: ARTICLE
Abstract: In this paper we study the viability of extending, to the general rotating electric machine's model, the passivity-based controller method that we have developed for induction motors. In this approach the passivity (energy dissipation) properties of the motor are taken advantage of at two different levels. First, we prove that the motor model can be decomposed as the feedback interconnection of two passive subsystems, which can essentially be identified with the electrical and mechanical dynamics. Then, we design a torque tracking controller that preserves passivity for the electrical subsystem, and leave the mechanical part as a ''passive disturbance''. In position or **speed** control applications this procedure naturally leads to the well known **cascaded** controller structure which is typically analyzed invoking time-scale separation assumptions. A key feature of the new cascaded control paradigm is that the latter arguments are obviated in the stability analysis. Our objective in this paper is to characterize a class of machines for which such a passivity-based controller solves the output feedback torque tracking problem. Roughly speaking, the class consists of machines whose nonactuated dynamics are well damped and whose electrical and mechanical dynamics can be suitably decoupled via a coordinate transformation. The first condition translates into the requirement of approximate knowledge of the rotor resistances to avoid the heed of injecting high gain into the loop. The latter condition is known in the electric machines literature as Blondel-Park transformability, and in practical terms it requires that the air-gap magnetomotive force must be suitably approximated by the first harmonic in its Fourier expansion. These conditions, stemming from the construction of the machine, have a clear physical interpretation in terms of the couplings between its electrical, magnetic and mechanical dynamics, and are satisfied by a large number of practical machines. The passivity-based controller presented here reduces to the well known indirect vector controller for current-fed induction machines. Our developments constitute an extension, to voltage-fed machines, of this de facto standard in industrial applications. Furthermore, our analysis provides it with a solid theoretical foundation.

21/7/36 (Item 1 from file: 35)

01505902 ORDER NO: AADMM-07712
TIMING OPTIMIZATION FOR HIERARCHICAL FIELD PROGRAMMABLE GATE ARRAYS
Author: CHAN, VI CUONG
Degree: M.A.SC.
Year: 1995
Corporate Source/Institution: UNIVERSITY OF TORONTO (CANADA) (0779)
Adviser: DAVID M. LEWIS
Source: VOLUME 34/05 of MASTERS ABSTRACTS.
PAGE 2020. 93 PAGES
ISBN: 0-612-07712-8

Field Programmable Gate Arrays are frequently used to implement complex multilevel digital circuits. This thesis investigates the methods for improving the **speed** of **Hierarchical** FPGA (HFPGA) architecture over conventional symmetrical FPGA. In a previous study (1), it was demonstrated

that the HFPGAs can be implemented with partially populated switch matrices and achieve lower switch counts than symmetrical FPGAs. This thesis extends that work by exploring timing issues.

By using the timing driven **placement** tool and direct **interconnect** optimization tool developed, we measured the performance of HFPGAs and symmetrical FPGAs using data gathered from experiments on a subset of benchmark circuits from the Microelectronics Centre of North Carolina (MCNC) (2). The results indicate that circuits using HFPGAs have better speed and area performance than those using symmetrical FPGAs. Furthermore, the experiments reveal that the use of direct interconnects can reduce the routing switch requirement and provide significant improvement on circuit speed at the same time.

21/7/37 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01470223 ORDER NO: AADAA-I9607096
VIRTUAL CELL IN MOBILE COMPUTER COMMUNICATIONS (WIRELESS NETWORKS)
Author: LIM, KYUNGSHIK
Degree: PH.D.
Year: 1994
Corporate Source/Institution: UNIVERSITY OF FLORIDA (0070)
Chairperson: YANN-HANG LEE
Source: VOLUME 56/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 6233. 116 PAGES

In this research, we design and develop a virtual cell approach for the transmission of IP datagrams in mobile computer communications. A virtual cell consists of a group of physical cells whose base stations are implemented by remote bridges and interconnected via high- **speed** datagram packet-switched networks. Host mobility is supported at the data **link** layer using the distributed **hierarchical location** information of mobile hosts. It eliminates the necessity of IP-level mobile host protocols that may interfere with the conventional IP protocol in a practical sense and achieves a logically flexible coverage area according to mobility and communication patterns among physical cells.

Given mobility and communication patterns among physical cells, the problem of deploying virtual cells is transformed to the optimization problem of finding a cover of disjoint clusters of physical cells. The objective is to minimize the total communication cost for the entire system where intercluster communication is more expensive than intracluster communication. Our problem differs from general graph partitioning problems in that it must meet the underlying topology constraints, such as the linear arrangement of physical cells in highway cellular systems and the hexagonal mesh arrangement of physical cells in cellular systems.

For highway cellular systems, we design an efficient optimal partitioning algorithm of $O(mn\sp2)$ by dynamic programming, where m is the number of clusters in a partition and n is the number of base stations. For hexagonal cellular systems, we develop several heuristics for multiway partitioning, based on the techniques of moving or interchanging boundary nodes between adjacent clusters. These heuristics produce optimal partitions with respect to the initial partitions obtained randomly or by centering. The heuristics are compared and shown to behave quite well through experimental testing and analysis.

Once an optimal partition of disjoint clusters is obtained, we can deploy the virtual cell system according to the topology of the optimal partition such that a cluster corresponds to a virtual cell. To analyze the performance of a virtual cell system, we adopt an open multiple class queueing network model. In addition to mobility and communication patterns

among physical cells, the topology of the virtual cell system is used to determine service transition probabilities of the queueing network model. By solving the traffic equations of the queueing network model, we obtain various performance measures such as the network response time for each type of message and the utilization of the base station networks and the backbone network of the virtual cell system.

21/7/38 (Item 3 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01469649 ORDER NO: AADAA-I9605990
WAVE EQUATION DIFFERENCE ENGINE (SEISMIC MODELING, COMPUTE ENGINE, MEMORY GAP)
Author: BORDING, RALPH PHILLIP
Degree: PH.D.
Year: 1995
Corporate Source/Institution: THE UNIVERSITY OF TULSA (0236)
Director: J. C. DIAZ
Source: VOLUME 56/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 6220. 79 PAGES

In this dissertation we report on the design, analysis, and construction of a wave equation difference engine. The complexity of wave propagation is sufficient to warrant the construction of a compute engine solely to generate model results. Model based seismic inversion methods can benefit from more powerful modeling methods. The approach used here is to provide a dedicated hardware solution. A second order finite difference algorithm for generation of synthetic acoustic waves is transformed into a wave equation difference engine. This hardware design exploits the expanding memory gap. The memory gap is the difference between slower memory cycle times and the increasingly faster processor **speeds** .

The kernel of the algorithm is transformed into an instruction **tree** . These complex instruction **trees** execute parallel arithmetic operations and are capable of generating multiple results. A memory design provides an independent memory structure for each array. The register **interconnection** is **organized** so the memory operates continuously. A prototype was constructed with four processors which operate in parallel. The system design is scalable without any loss of efficiency. Seismic modeling results from the wave equation difference engine are presented.

21/7/39 (Item 4 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01269387 ORDER NO: NOT AVAILABLE FROM UNIVERSITY MICROFILMS INT'L.
DATA STRUCTURES FOR GRAPHICAL INFORMATION IN CAD
Original Title: DATASTRUKTUREN VOOR GRAFISCHE INFORMATIE BIJ CAD

Author: DE PAUW, WIM
Degree: DR.
Year: 1991
Corporate Source/Institution: RIJKSUNIVERSITEIT TE GENT (BELGIUM) (0215)
Source: VOLUME 54/01-C OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 303. 276 PAGES
Language: DUTCH
Location of Reference Copy: LABORATORY OF ELECTRONICS, ST. PIETERSNIEUWSTR. 41, B-9000 GENT, BELGIUM

The demand for powerful CAD programs, handling large amounts of geometric data, is continuously growing. The physical layout for VLSI circuits for example, may constist of more than one million rectangles. Clearly, these data need a special organization in order to allow fast queries.

Using a simple **organization** , such as a **linked list** , a region query would take O(N) time. Very often, a balance has to be made between the memory requirements and the speed that can be obtained for basic operations, such as insertions and searches.

First, a performance prediction is proposed for Multiple Storage Quad **Trees** , a well known data structure. Practical characteristics, such as memory usage and the **speed** of query operations can be obtained.

In a new data structure, Multiple Storage Adaptive Multitrees, we use a variable branching factor throughout the **tree** . A simple scheme was presented to adjust this branching factor to the local characteristics of the layout. **Speed** for queries in large areas was improved using a technique, Four List Quad **Trees** , using four different list types for the storage of objects. The combination of the two above mentioned techniques leads to the Four List Adaptive Multitrees structure. This data structure is very fast for region queries and insertion operations, while keeping memory requirements low. We finally developed a data structure, Quad **Trees** with Internal Storage. For this data structure, the concept of internal object lists was presented. It **speeds** up access and insertion for large objects. It has the additional advantage of reducing storage space.

21/7/40 (Item 1 from file: 94)

01395385 JICST ACCESSION NUMBER: 91A0810683 FILE SEGMENT: JICST-E

Special Issue on LAN: High Speed **, Multimedia, and Reliability. Considerations on the Design Methods of** Hierarchical **Large-Scale Local Area Networks.**

SAKATA M (1); NEMOTO Y (1); NOGUCHI S (1)
(1) Tohoku Univ., Sendai-shi, JPN

IEICE Trans(Inst Electron Inf Commun Eng), 1991, VOL.E74,NO.9, PAGE.2747-2755, FIG.8, TBL.5, REF.20
JOURNAL NUMBER: F0699BCQ ISSN NO: 0917-1673
UNIVERSAL DECIMAL CLASSIFICATION: 681.3:654
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

ABSTRACT: Tohoku University has been constructing the academic information-exchange network TAINS (Tohoku University Academic/All-round/Advanced Information Network System) to link its widely spread campuses and to meet several demands for an intrauniversity network. TAINS, the first network based on OSI, became operational in April 1988. The primary function of TAINS is to **connect** all the geographically dispersed **locations** of the university via a high-speed digital network in order to facilitate an easy and efficient interconnection among the various computers, terminals and other scientific equipment. TAINS is constructed as a large-scale local area network of hierarchical sturucture. In the hierarchical network of TAINS, a backbone network, consisting of two 100 Mbps cptical fiber rings, interconnects several small-scale IEEE802.3 networks, each of which span a building or a part of a building. This paper describes the background, the basic design concept and the constitution of TAINS. In

TAINS, the inhouse network protocol is OSI-based, and the ring network protocol is based on FDDI. The use of these communication protocols are reviewed and the protocol matching adopted for TAINS is described. Finally, a method for estimating the stable operation of a 2-layer hierarchical network using traffic analysis is given. (author abst.)

21/7/41 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00935308 E95116362062
Cost comparison of STM and ATM transport networks
(Kostenvergleich der STM- und ATM-Transportnetze)
Hadama, H; Izaki, T; TokizawaI
NTT Transmission Syst. Lab., Kanagawa, J
Networks 94, Planning for a Customer Responsive Network, 6th Internat. Planning Symp., Proc., Budapest, H, Sep 4-9, 19941994
Document type: Conference paper Language: English
Record type: Abstract

ABSTRACT:
Path network installation costs for B-ISDN infrastructures were discussed. The virtual path scheme in ATM networks has many desirable features such as non-deterministic path capacity, non- **hierarchical** path configuration, and direct multiplexing capability into high **speed** transmisson links. These merits enable network providers to create the minimum link cost path network without significantly increasing cross connect costs (i.e. node costs). Quantitative evaluations show that the virtual path scheme can attain a more cost effective path network than the digital path schemes based on STM. This paper assumed that the cross **connect** function was **placed** at every node in order to realize sophisticated path control functions such as path route alteration for failure restoration, and flexible path rearrangement to meet demand. A detailed ATM introduction strategy, which would address the local network and the subscriber line network, and optimization of ATMXC location, considering not only installation costs, but also path layer operability, are for further study.

21/7/42 (Item 2 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00928035 I95093732352
Executing algorithms with hypercube topology on torus multicomputers
(Ausfuehrung von Parallelalgorithmen in einer Hypercube-Topologie auf Multicomputern mit einer Torus-Verbindungsstruktur)
Gonzalez, A; Valero-Garcia, M; Diaz de Cerio, L
Dept. d'Arquitectura de Computadors, Univ. Politecnica de Catalunya, Barcelona, Spain
IEEE Transactions on Parallel and Distributed Systems, v6, n8, pp803-814, 1995
Document type: journal article Language: English
Record type: Abstract
ISSN: 1045-9219

ABSTRACT:
Many parallel algorithms use hypercubes as the communication topology among their processes. When such algorithms are executed on hypercube multicomputers the communication cost is kept minimum since processes can be allocated to processors in such a way that only communication between

neighbor processors is required. However, the scalability of hypercube multicomputers is constrained by the fact that the interconnection cost-per-node increases with the total **number** of **nodes** . From scalability point of view, meshes and toruses are more interesting classes of interconnection **topologies** . This paper focuses on the execution of algorithms with hypercube communication topology on multicomputers with mesh or torus interconnection topologies. The proposed approach is based on looking at different embeddings of hypercube graphs onto mesh or torus graphs. The paper concentrates on toruses since an already known embedding, which is called standard embedding, is optimal for meshes. In this paper, an embedding of hypercubes onto toruses of any given dimension is proposed. This novel embedding is called xor embedding. The paper presents a set of performance figures for both the standard and the xor embeddings and shows that the latter outperforms the former for any torus. In addition, it is proven that for a one-dimensional torus (a ring) the xor embedding is optimal in the sense that it minimizes the execution time of a class of parallel algorithms with hypercube topology. This class of algorithms is frequently found in real applications, such as FFT and some class of sorting algorithms.

21/7/43 (Item 3 from file: 95)

00581058 I92038092937
Vibration control of a two-link flexible robot arm
(Schwingungsfreie Feinregelung der Lageregelung eines zweifach verbundenen Roboterarmes)
Hillsley, KL; Yurkovich, S
Dept. of Electr. Eng., Ohio State Univ., Columbus, OH, USA
Proceedings. 1991 IEEE International Conference on Robotics and Automation, 9-11 April 1991, Sacramento, CA, USA1991
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 0-8186-2163-X

ABSTRACT:
Analysis and experimentation are described for a two-link apparatus in which both members are very flexible. Attention is focused on endpoint position control for point-to-point movements, assuming a fixed reference frame for the base, with two rotary joints. Each link in instrumented with acceleration sensing and is driven by a separate motor equipped with velocity and position sensing. The control perspective adopted is to implement a two-stage control in which the vibration control problem for fine motion endpoint positioning is considered separately from the gross motion, large angle skew problem. In the first stage the control law shapes the actuator inputs for the large angle movement in such a way that minimal energy is injected into the flexible modes, while in the second phase an endpoint acceleration feedback scheme is employed in independent joint control for vibration suppression at the link endpoints.

21/7/44 (Item 4 from file: 95)

00563734 I91123666928
Product forms for random access schemes
(Produktformen fuer Direktzugriffsschemata)
Dijk, NMvan

Free Univ., Fac. of Econ. & Econometries, Amsterdam, Netherlands
Computer Networks and ISDN Systems, v22, n4, pp303-317, 1991
Document type: journal article Language: English
Record type: Abstract
ISSN: 0169-7552

ABSTRACT:
A unifying framework is presented to conclude explicit product form expressions for the steady state distribution of busy sources (transmitters, lines) for random access communication protocols. Transmission times and packet lengths are generally distributed. The main results are: an insensitive product form expression; a concrete condition in terms of system protocols; and a generalization of product form random access protocols. These results unify and extend known results. Particularly it includes CSMA protocols with non-exponential transmissions and packets, state dependent transmission **speeds** , and link selective characteristics. A variety of 'novel' examples is given such as with **hierarchical** circuit switching, synchronous serving, randomized grading, message **priorities** , error probabilities, **link** selective transmissions and an extension of rude CSMA.

21/7/45 (Item 5 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00562761 I92013655928
Considerations on the design methods of hierarchical large-scale local area networks
(Entwurfsverfahren fuer hierarchisch strukturierte, grosse lokale Netze)
Sakata, M; Nemoto, Y; Noguchi, S
Comput. Center, Tohoku Univ., Sendai, Japan
1991
Document type: journal article Language: English
Record type: Abstract

ABSTRACT:
The academic information-exchange network TAINS (Tohoku University Academic/All-round/Advanced Information Network System) has been introduced to link widely spread campuses and to meet several demands for an intrauniversity network. TAINS, the first network based on OSI, became operational in April 1988. The primary function of TAINS is to **connect** all the geographically dispersed **locations** of the university via a high-speed digital network in order to facilitate an easy and efficient interconnection among the various computers, terminals and other scientific equipment. TAINS is constructed as a large-scale local area network of hierarchical structure. In the hierarchical network of TAINS, a backbone network consisting of two 100 Mbps optical fiber rings interconnects several small-scale IEEE802.3 networks each of which span a building or a part of a building. This paper describes the background, the basic design concept and the constitution of TAINS. In TAINS, the inhouse network protocol is OSI-based, and the ring network protocol is based on FDDI. The use of these communication protocols is reviewed and the protocol matching adopted for TAINS is described. Finally, a method for estimating the stable operation of a two-layer hierarchical network using traffic analysis is given.

21/7/46 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1519770 H.W. WILSON RECORD NUMBER: BAST97032390

The Fibonacci heap

Boyer, John;

Dr. Dobb's Journal v. 22 (Jan. '97) p. 106-8+
DOCUMENT TYPE: Feature Article ISSN: 1044-789X

ABSTRACT: The Fibonacci heap, or F-heap, uses a roughly balanced **tree** of circularly **linked lists** to perform DecreaseKey() and Insert() operations at exceptionally high **speeds** . Although the Fibonacci heap only requires constant time for these operations, it has the disadvantage of requiring more memory than a binary heap and the drawback of basing the time efficiency of the different operations on "amortized analysis." A detailed description of the Fibonacci heap is given, and the Fibonacci heap and the binary heap are compared.

```
File 348:EUROPEAN PATENTS 1978-2003/Jun W01
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030612,UT=20030605
         (c) 2003 WIPO/Univentio
? ds

Set     Items   Description
S1     150752   TREE OR TREES OR HIERARCH? OR TREEMAP? OR GRID OR GRIDS OR
             TOPOLOG?????? ? OR PYRAMID? ? OR CASCAD? OR SUBTREE? ?
S2      70982   PARENT? ? OR CHILD OR CHILDREN
S3     350809   SPEED OR SPEEDS
S4       7732   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (PORT OR PORTS)
S5       6315   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (NODE OR NODES)
S6     287211   PRIORIT? OR RANK???? ?
S7      71008   SORT OR SORTS OR SORTED OR SORTING?
S8     223820   ORGANIS? OR ORGANIZ?
S9    1271063   PLACE? ? OR PLACING? OR PLACEMENT? OR PLACED OR POSITION???
              ? OR LOCAT???? ? OR LIST OR LISTS OR LISTED OR LISTING? ? OR
             SITUATE? ? OR SITUATING OR SITED
S10    143618   S6:S9(5N)(CONNECT? OR INTERCONNECT? OR LINK??? ? OR INTERL-
             INK?)
S11    129666   S3:S5(S)S6:S9
S12      3304   S11(S)S1:S2
S13      5031   S3:S5(20N)S1:S2
S14       117   S13(S)S10
S15        17   S14/TI,AB,CM
S16      2165   S3:S5(20N)S10
S17        98   S16(S)S1:S2
S18        10   S17/TI,AB,CM
S19     73158   S3:S5(20N)S6:S9
S20       842   S19(20N)S1:S2
S21        78   S20(S)S10
S22        10   S21/TI,AB,CM
S23      6493   IC='G06F-001/':IC='G06F-001/00'
S24        36   IC='G06F-000/00':IC='G06F-000/15'
S25      4281   IC='H04L-012/28'
S26       581   IC='G06F-013/14'
S27       180   S14 OR S17 OR S21
S28         6   S27 AND S25
S29         2   S27 AND (S23:S24 OR S26)
S30        28   S15 OR S18 OR S22 OR S28:S29
S31        28   IDPAT (sorted in duplicate/non-duplicate order)
S32        28   IDPAT (primary/non-duplicate records only)
? t32/5,k/all

 32/5,K/1     (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

01067115
```
Data communication system data communication method and data communication apparatus

Datenkommunikationssystem, Datenkommunikationsverfahren, Datenkommunikation svorrichtung und digitale Schnittstelle

Systeme de communication de donnees, methode de communication de donnees, dispositif de communication de donnees et interface numerique

```
PATENT ASSIGNEE:
  CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku,
    Tokyo, (JP), (Applicant designated States: all)
```

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Ohnishi, Shinji, Canon Kabushiki Kaisha, 30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 939530 A2 990901 (Basic)
APPLICATION (CC, No, Date): EP 99301316 990223;
PRIORITY (CC, No, Date): JP 9842656 980224; JP 9861708 980312; JP 9884709 980330
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H04L-029/06; **H04L-012/28** ; H04B-001/20

ABSTRACT EP 939530 A2
A data communication system comprises devices having at least the functions of a source, a destination, and a controller. The source transmits information data by using an address specifying one part of a memory space provided in a destination. The destination stores the information data in one part of the memory space specified by that address. The controller manages data transmission between the source and the destination. In a data communication system such as this, at least one device from among the source, the destination, and the controller resumes transmission of the information data without discarding any part of the data stored in the memory space, in the event that the transmission of the information data is interrupted in conformance with the default settings of a network.
ABSTRACT WORD COUNT: 128
NOTE:
Figure number on first page: 2

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 990901 A2 Published application without search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9935	1193
SPEC A	(English)	9935	16302
Total word count - document A			17495
Total word count - document B			0
Total word count - documents A + B			17495

...INTERNATIONAL PATENT CLASS: **H04L-012/28**

...SPECIFICATION communication system begins automatically. Basically, node IDs are specified by the node with the higher **hierarchical** position allowing a physical address to be specified for a node with a lower **hierarchical position** which is **connected** to a communication port with a lower **port number** , following which the lower- **position** node grants permission for its own subsidiary nodes to specify addresses, and the processing continues...communication system begins automatically. Basically, node IDs are specified by the node with the higher **hierarchical** position allowing a physical address to be specified for a node with a lower **hierarchical position** which is **connected** to a

communication port with a lower **port number** , following which the lower- **position** node grants permission for its own subsidiary nodes to specify addresses, and the processing continues...

32/5,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01056289
Methods, systems and apparatus for providing device identification within a network
Verfahren, Systemen und Vorrichtung zum Beschaffen von Gerateidentifikation in einem Netzen
Methodes, systemes et dispositif pour fournir une identification a un equipement dans un reseau
PATENT ASSIGNEE:
Sony Electronics Inc., (1360226), One Sony Drive, Park Ridge, New Jersey 07656, (US), (applicant designated states: AT;BE;CH;CY;DE;DK;ES;FI;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)
INVENTOR:
Ogino, Hiroshi, 730 East Evelyn Ave. No 624, Sunnyvale, California 94086, (US)
Zou, Feng (Frank), 1775 Milmont Drive, Apartment No. E201, Milpitas, California 95035, (US)
LEGAL REPRESENTATIVE:
Pilch, Adam John Michael (50481), D. YOUNG & CO., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 932275 A2 990728 (Basic)
APPLICATION (CC, No, Date): EP 99300097 990106;
PRIORITY (CC, No, Date): US 3111 980106
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: **H04L-012/28** ; H04L-029/12

ABSTRACT EP 932275 A2
A method and system for providing a device identification mechanism within a consumer electronics based audio/video network. Several consumer electronics products, e.g., television, VCR, tuner, set-top box (e.g. intelligent receiver/decoder, IRD), DVTRs, PCs, DVD players (digital video disk), etc., can be coupled within the network to communicate together via a standard bus, such as an IEEE 1394 serial communication bus (30). In one embodiment, the HAVI network offers unique advantages to consumer electronic vendors because the architecture offers for the home network many of the advantages of existing computer system networks. Specifically, interconnected devices can share resources and provide open, well defined APIs that allow ease of development for third party developers. A global unique identifier (GUID) is associated with each device (e.g. 20) of the HAVI network. A low level driver (320) constructs a GUID list (510) of each device on the HAVI network. The order of the GUID entries in the GUID list (e.g., the index) matches the physical identifiers assigned to the devices by the 1394 serial bus (30). Although the physical identifiers can change on bus reset, the GUID values are constant and are used for device communication. Speed map (515) and topology map (520) information is maintained based on the physical identifier information and therefore translations between GUIDs and physical identifiers are efficiently performed when referencing speed map and topology information for an application.
ABSTRACT WORD COUNT: 230

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 990728 A2 Published application (A1with Search Report ;A2without Search Report)
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9930	1892
SPEC A	(English)	9930	14580
Total word count - document A			16472
Total word count - document B			0
Total word count - documents A + B			16472

INTERNATIONAL PATENT CLASS: **H04L-012/28** ...

...SPECIFICATION GUID) is associated with each device of the HAVI network. A low level driver, a **link** driver, constructs a GUID **list** including a GUID for each device on the HAVI network. The order of the GUID...

...Within the present invention, network-based applications use a device's GUID to communicate therewith. **Speed** map and **topology** map information is maintained based on the physical identifier information. Therefore translations between GUIDs and physical identifiers are efficiently performed by the present invention and are used for referencing **speed** map and **topology** information for an application program or other object.

The 1394 local bus architecture creates a...1394 Bus Manager 370 is also shown. The CMM 250 contains a copy of the **speed** map 515 and the **topology** map 520 (described further below) and and IEEE 1394 Bus Manager 370 contains control/status...

...pending transactions and controls retry protocol operations with a busy/timeout register. Data transmission takes **place** within the **link** layer 380 and the I/F (CFR) unit 385.

DCM 230 AND DCM MANAGER 270...

32/5,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00930202
Device for cutting a strip-like package
Vorrichtung zum Schneiden einer Streifenverpacknung
Dispositif pour couper un emballage sous forme de bande
PATENT ASSIGNEE:
Bayer Bitterfeld GmbH, (2235650), Salegaster Chaussee 1, 06803 Greppin, (DE), (Proprietor designated states: all)
INVENTOR:
Scharbrodt, Paul, Saarstrasse 11, 51375 Leverkusen, (DE)
Feja, Siegbert, Nordring 9, 06766 Wolfen, (DE)
Hoffmann, Eckhard, Otto-Schmidt-Strasse 27, 06766 Wolfen, (DE)
LEGAL REPRESENTATIVE:
Drope, Rudiger, Dr. et al (47043), Bayer AG Konzernbereich RP Patente und Lizenzen, 51368 Leverkusen, (DE)
PATENT (CC, No, Kind, Date): EP 847926 A1 980617 (Basic)
EP 847926 B1 000809
APPLICATION (CC, No, Date): EP 97121053 971201;
PRIORITY (CC, No, Date): DE 19651954 961213
DESIGNATED STATES: CH; DE; ES; FR; GB; IT; LI

Change: 990804 A2 Title of invention (German) (change)
Change: 990804 A2 Title of invention (English) (change)
Change: 990804 A2 Title of invention (French) (change)
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200019	3628
CLAIMS B	(German)	200019	3277
CLAIMS B	(French)	200019	4728
SPEC B	(English)	200019	23000
Total word count - document A			0
Total word count - document B			34633
Total word count - documents A + B			34633

32/5,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00662133
Method and apparatus for an automatic decomposition of a network topology into a backbone and subareas
Verfahren und Gerat zur automatischen Verteilung einer Netztopologie in Haupt- und Nebentopologie
Methode et appareil de decomposition automatique d'une topologie de reseau en topologie principale et sous aire
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (Proprietor designated states: all)
INVENTOR:
Galand, Claude, 56, avenue des Tuilieres, F-06800 Cagnes Sur Mer, (FR)
Scotton, Paolo, 1561, Chemin de Ste Colombe, F-06140 Vence, (FR)
LEGAL REPRESENTATIVE:
de Pena, Alain (15151), Compagnie IBM France Departement de Propriete Intellectuelle, 06610 La Gaude, (FR)
PATENT (CC, No, Kind, Date): EP 637153 A1 950201 (Basic)
EP 637153 B1 011031
APPLICATION (CC, No, Date): EP 93480105 930730;
PRIORITY (CC, No, Date): EP 93480105 930730
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: H04L-012/56
CITED REFERENCES (EP B):
COMPUTER NETWORKS. vol. 1 , 1977 , AMSTERDAM NL pages 155 - 174 L.KLEINROCK ET AL 'HIERARCHICAL ROUTING FOR LARGE NETWORKS'
IEEE TRANSACTIONS ON COMPUTERS vol. 38, no. 8 , August 1989 , NEW YORK US pages 1059 - 1074 XP47576 W.T.TSAI ET AL 'AN ADAPTIVE HIERARCHICAL ROUTING PROTOCOL'
IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATION. vol. 7, no. 8 , October 1989 , NEW YORK US pages 1243 - 1252 XP126342 V.R.SAKSENA 'TOPOLOGICAL ANALYSIS OF PACKET NETWORKS';

ABSTRACT EP 637153 A1
The object of the invention is to perform an automatic decomposition of a packet switching network in backbone nodes and subareas nodes to speed up the routing path search without degrading the optimization criterion of the routing algorithm and without generating additional control messages on the network.
Currently, routing algorithms compute all the available paths in the network, from the source node to the destination node before to select an optimal route. However, networks are rarely fully meshed. They are usually built around a hierarchical structure : a set of nodes,

interconnected by high throughput lines, are used to build a backbone with a high degree of meshing and then, local nodes are grouped in geographical subareas themselves attached to the backbone. Routing algorithms can take advantage of this particular network topology to drastically reduce the complexity of paths computation. For a given connection, only a limited number of nodes are defined as usable and are taken in account by the algorithm in its path calculation. (see image in original document)

ABSTRACT WORD COUNT: 173

NOTE:

Figure number on first page: 8

LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant:	011031	B1	Granted patent
Application:	950201	A1	Published application (A1with Search Report ;A2without Search Report)
Lapse:	030226	B1	Date of lapse of European Patent in a contracting state (Country, date): NL 20011031, SE 20020131, BE 20011031, AT 20011031,
Lapse:	030205	B1	Date of lapse of European Patent in a contracting state (Country, date): SE 20020131, BE 20011031,
Lapse:	020626	B1	Date of lapse of European Patent in a contracting state (Country, date): SE 20020131,
Oppn None:	021023	B1	No opposition filed: 20020801
Lapse:	030219	B1	Date of lapse of European Patent in a contracting state (Country, date): NL 20011031, SE 20020131, BE 20011031,
Examination:	950719	A1	Date of filing of request for examination: 950519
*Assignee:	970205	A1	Applicant (transfer of rights) (change): International Business Machines Corporation (200120) Old Orchard Road Armonk, N.Y. 10504 (US) (applicant designated states: AT;BE;CH;DE;ES;FR;GB;IT;LI;NL;SE)
Examination:	991110	A1	Date of dispatch of the first examination report: 19990924

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	1175
CLAIMS B	(English)	200144	590
CLAIMS B	(German)	200144	595
CLAIMS B	(French)	200144	706
SPEC A	(English)	EPABF2	8480
SPEC B	(English)	200144	9679
Total word count - document A			9657
Total word count - document B			11570
Total word count - documents A + B			21227

...CLAIMS backbone between the pair of subareas, the backbone path including a link to each subarea **interconnected** through the highest **ranked** node from the set of nodes connecting the two links;

* removing from the set of...

...any link in which the parent node in the subarea is not connected to the **parent** in the backbone and any link to a subarea having less than a predetermined **number** of **nodes** ;

* storing data representing the sets of links selected by said

substantially the same diameter as the outside diameter of the **parent** bar. The joining mechanism does not require a separate component or sleeve to join the bolts together but is formed from the material of the **parent** bar lengths. The joining mechanism is a high- **speed** connection, which reduces handling and installation times and ensures that the engagement of mating threads is fully in **place** . The high- **speed connection** is a mating male and female thread of right or left-hand thread depending on...3o The male end portion 20 and socket end portion 21 are formed from the **parent** deformed bar by a multi-

32/5,K/8 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00952986 **Image available**
PROTOCOL AND STRUCTURE FOR SELF-ORGANIZING NETWORK
PROTOCOLE ET STRUCTURE POUR RESEAU AUTO-ORGANISE
Patent Applicant/Assignee:
MOTOROLA INC, 1303 East Algonquin Road, Schaumburg, IL 60196, US, US (Residence), US (Nationality)
Inventor(s):
MAEDA Masahiro, 4-6-18-401 Ogikubo, Suginami-ku, Tokyo 167-0051, JP,
BOURGEOIS Monique, 729 N.W. 91st Terrace, Plantation, FL 33324, US,
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CHEN Priscilla, 7661 N.W. 42nd Place, #274, Sunrise, FL 33351, US,
HUANG Jian, 431 N.W. 118th Way, Coral Springs, FL 33071, US,
HUANG Yan, 9664 N.W. 7th Circle, #1224, Plantation, FL 33324, US,
SHI Qicai, 5462 N.W. 122 Drive, Coral Springs, FL 33076, US,
Legal Representative:
FULLER Andrew S (et al) (agent), 8000 West Sunrise Blvd., Room 1610, Fort Lauderdale, FL 33322, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200287172 A1 20021031 (WO 0287172)
Application: WO 2002US12519 20020419 (PCT/WO US0212519)
Priority Application: US 2001285165 20010420
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **H04L-012/28**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 10365

English Abstract
The method of self-organization includes processes for cluster (Fig. 2) formation, network maintenance, intra-cluster communication (Fig. 1). In the cluster formation process, each node discovers if any neighboring node (9, 8, 11) is a cluster head or if any node is already a member of a cluster, and if a cluster head or a networked node is discovered, each node establishes a communication link with the cluster head or the networked node. If no cluster head or networked node is discovered, the

node itself becomes a cluster head. The network is maintained by each node periodically broadcasting a HELLO message to neighboring nodes (Fig. 6), receiving responses the message and updating a neighbour list in accordance with responses to the HELLO message. The resulting network has one or more clusters of nodes, each with a cluster head and a number of member nodes, each assigned a node identifier by the cluster head. Border nodes are members of at least two clusters acting as routers.

French Abstract

Selon l'invention, le procede d'auto-organisation comprend des processus de formation de groupes (fig.2), de mise a jour de reseau, de communications intra-groupe (fig.1). Dans le processus de formation de groupes, chaque noeud decouvre si un quelconque noeud voisin (9, 8, 11) est une tete de groupe ou deja membre d'un groupe et, si une tete de groupe ou un noeud en reseau est decouvert, chaque noeud etablit une liaison de communication avec ladite tete de groupe ou ledit noeud en reseau. Si on ne decouvre aucune tete de groupe, ni aucun noeud en reseau, le noeud lui-meme devient tete de groupe. Le reseau est mis a jour par chaque noeud diffusant regulierement un message d'accueil a destination des noeuds voisins (fig.6), recevant des reponses a ce message d'accueil et mettant a jour une liste de voisinage en fonction des reponses au messages d'accueil. Le reseau resultant possede au moins un groupe de noeuds, chacun avec une tete de groupe et plusieurs noeuds membres, auxquels la tete de groupe attribue un identificateur de noeud. Les noeuds frontieres sont membres d'au moins deux groupe faisant office de routeurs.

Legal Status (Type, Date, Text)
Publication 20021031 A1 With international search report.
Publication 20021031 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
Examination 20030403 Request for preliminary examination prior to end of 19th month from priority date

Main International Patent Class: **H04L-012/28**
Fulltext Availability:
Claims

Claim
... 40, wherein the process of cluster maintenance further comprises:
the cluster head generating a topology **list** based upon one or more **link** -state reports received from neighboring nodes; and
the cluster head sending a **TOPOLOGY** LTDATE message to neighboring nodes.

42 A method in accordance with claim 40, wherein the **topology list** is generated by selecting the route between the cluster head and a neighboring node that uses the smallest **number** of **nodes** .

43 A method in accordance with claim 41, wherein the process of cluster maintenance further comprises updating the **topology list** if the node fails to send a link-state report

32/5,K/9 (Item 9 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00935341 **Image available**

METHODS AND APPARATUS FOR NETWORK ROUTING DEVICE

PROCEDES ET SYSTEME UTILES POUR DISPOSITIF DE ROUTAGE DE RESEAU

Patent Applicant/Assignee:
GOTHAM NETWORKS INC, 15 Discovery Way, Acton, MA 01720, US, US (Residence), US (Nationality)

Inventor(s):
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BEARDSLEY Alan, 23 Loomis Street, Bedford, MA 01730, US,
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Legal Representative:
POWSNER David J (et al) (agent), Nutter, McClennen & Fish LLP, One International Place, Boston, MA 02110-2699, US,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200269575 A1 20020906 (WO 0269575)
Application: WO 2002US6299 20020228 (PCT/WO US0206299)
Priority Application: US 2001272328 20010228; US 2001272387 20010228; US 2001272407 20010228

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: **H04L-012/28**
International Patent Class: H04L-012/56; H04J-003/24
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 18592

English Abstract

The present invention provides systems for improved quality of service and traffic management in network routers and other devices. This is achieved by coupling a plurality of queue processors to a plurality of input interfaces (18) that receive data from one or more respective network connections (12). Each queue processor, in coordination with an associated scheduler (24) that schedules dequeing of data from one or more queues (22), maintains with quality of service levels with respect to throughput, and delivers the data for a particular output context based on priority to a respective output interface (26). Packets, cell, datagrams and so forth passing through the router are disassembled and marked with one or more priority levels. Prior to exiting the router they are reassembled according to marked priority levels into their constituent forms for continued routing on the network.

French Abstract

L'invention concerne des systemes permettant d'ameliorer la qualite de service et la gestion de trafic ameliorees dans des routeurs de reseau, entre autres. Pour ce faire, une pluralite de processeurs de file d'attente sont couples a une pluralite d'interfaces (18) d'entree qui recoivent des donnees provenant d'une ou de plusieurs connexions (12) de reseau respectives. Chaque processeur de file d'attente, en coordination avec un ordonnanceur (24) associe qui ordonnance le retrait de donnees d'une ou de plusieurs files (22) d'attente, maintient des niveaux de

qualite de service par rapport au debit et remet lesdites donnees a une interface (26) de sortie respective dans un contexte de sortie particulier en fonction de leur priorite. Les paquets, cellules, datagrammes etc. qui passent par le routeur sont desassembles et marques d'un ou de plusieurs niveaux de priorite. Avant de sortir du routeur, ils sont reassembles, selon les niveaux de priorite marques, en leurs formes constitutives en vue de la continuation du routage sur le reseau.

Legal Status (Type, Date, Text)
Publication 20020906 A1 With international search report.
Publication 20020906 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

Main International Patent Class: **H04L-012/28**
Fulltext Availability:
Claims

Claim
... serviced by a single Global Scheduler. Data is stored in the QP Data Memory in **linked - list** fashion on logical queues. The total number of queues Nq is equal to the product of the **number** of logical **ports** being serviced by this card's egress interfaces times the number of priority levels supported...

32/5,K/10 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00911811 **Image available**
NETWORK ACCESS SYSTEM INCLUDING A PROGRAMMABLE ACCESS DEVICE HAVING DISTRIBUTED SERVICE CONTROL
SYSTEME D'ACCES AU RESEAU INCLUANT UN APPAREIL D'ACCES PROGRAMMABLE A COMMANDE DE SERVICES DISTRIBUES
Patent Applicant/Assignee:
WORLDCOM INC, 515 East Amite Street, Jackson, MS 39201, US, US (Residence), US (Nationality)
Inventor(s):
MCDYSAN Dave, 2159 Astoria Circle, #104, Herndon, VA 20170, US,
THOMAS Howard Lee, 325 Woodmar Court, Ballwin, MO 63011, US,
YAO Lei, 2000 S. Eads Street, #517, Arlington, VA 22202, US,
Legal Representative:
GROLZ Edward W (agent), Scully, Scott, Murphy & Presser, 400 Garden City Plaza, Garden City, NY 11530, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200245317 A2-A3 20020606 (WO 0245317)
Application: WO 2001US44398 20011128 (PCT/WO US0144398)
Priority Application: US 2000723482 20001128
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **H04L-012/28**
International Patent Class: H04L-012/56; G06F-015/16
Publication Language: English

Filing Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 18982

English Abstract
  A distributed network access system (30) in accordance with the present invention includes at least an external processor (42) and a programmable access device (40). The programmable access device has a message interface coupled to the external processor and first and second network interfaces through which packets are communicated with a network. The programmable access device includes a packet header filter and a forwarding table (50) that is utilized to route packets communicated between the first and second network interfaces. In response to receipt of a series of packets, the packet header filter in the programmable access device identifies messages in the series of messages upon which policy-based services are to be implemented and passes identified messages via the message interface to the external processor for processing. In response to receipt of a message, the external processor invokes service control on the message and may also invoke policy control (48) on the message.

French Abstract
  La presente invention concerne un systeme d'acces au reseau distribue incluant au moins un processeur externe et un appareil d'acces programmable. Cet appareil d'acces programmable comporte une interface messages couplee au processeur externe, ainsi que deux interfaces reseau permettant l'echange des paquets avec un reseau. L'appareil d'acces programmable comporte un filtre a en-tetes de paquets et une table de reacheminement qui sert a l'acheminement des paquets echanges entre les deux interfaces reseau. En reaction a la reception d'une serie de paquets, le filtre d'en-tetes de paquets de l'appareil d'acces programmable commence par identifier les messages dans la serie de messages pour lesquels on doit mettre en oeuvre des services a base de politique, puis remet en vue de traitement les messages identifies au processeur externe via l'interface messages. En reaction a la reception d'un message, le processeur externe sollicite la commande de service pour le message, tout en pouvant egalement solliciter la commande de politique pour ce meme message.

Legal Status (Type, Date, Text)
Publication 20020606 A2 Without international search report and to be republished upon receipt of that report.
Examination 20021121 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20030213 Late publication of international search report
Republication 20030213 A3 With international search report.

Main International Patent Class: **H04L-012/28**
Fulltext Availability:
  Detailed Description

Detailed Description
... As shown, PADs 40 may also be located at higher levels in the aggregation network **hierarchy** . Engineering economic and/or performan ce considerations determine **placement** of PADs 40.
For example, aggregation of a minimum amount of traffic or the need to access a low **speed** access **link** may drive **placement** of a PAD 40 to higher and lower access network levels, respectively.

detection employes dans de tels systemes. Chaque faisceau d'illumination laser planaire est produit a partir d'une matrice de faisceaux d'illumination laser planaire (PLIA) comprenant une pluralite de modules PLIM d'illumination par faisceau laser. Chaque PLIM est constitue d'une diode laser visible (VLD), d'une lentille de focalisation, et d'un element optique cylindrique monte en consequence. Chacun des composants du faisceau d'illumination laser planaire produit a partir de chacun des PLIM est soumis a une combinaison optique de facon a produire un faisceau d'illumination laser composite sensiblement planaire aux caracteristiques de densite de puissance sensiblement uniformes sur la totalite de son etendue spatiale, et donc sur la plage operationnelle du systeme. De preference, chaque composant du faisceau d'illumination laser planaire est focalise de facon a n'avoir qu'un minimum de largeur du faisceau au point ou sur le plan qui est a la plus grande distance de l'objet a laquelle le systeme est concu pour l'acquisition d'images, ce qui compense la perte de densite de puissance du faisceau incident d'illumination laser planaire en raison du fait que la largeur du faisceau d'illumination laser planaire augmente en longueur de facon a augmenter la distance par rapport a l'optique d'imagerie. Grace a la presente invention, il est maintenant possible d'utiliser des detecteurs image de type VLD et a cellule CCD grande vitesse dans des applications a bande transporteuse, douchette ou sous-table, tout en tirant profit des avantages que procure une telle technologie, tout en evitant les inconvenients qui s'y rattachaient jusqu'alors.

Legal Status (Type, Date, Text)
Publication 20020530 A2 Without international search report and to be republished upon receipt of that report.
Examination 20030116 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20030327 Late publication of international search report
Republication 20030327 A3 With international search report.

32/5,K/12 (Item 12 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00893956
PROJECT MANAGEMENT SYSTEM AND METHOD
PROCEDE ET SYSTEME DE GESTION DE PROJET
Patent Applicant/Assignee:
RESERVOIRTEAM LIMITED, 7th floor, Hillgate House, 26 Old Bailey, London EC4M 7HW, GB, GB (Residence), GB (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
HERWIGER Joost Christian, 3594 Nyland Way, Lafayette, CO 80026, US, US (Residence), NL (Nationality), (Designated only for: US)
Legal Representative:
REDDIE & GROSE (agent), 16 Theobalds Road, London WC1X 8PL, GB,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200226014 A2 20020404 (WO 0226014)
Application: WO 2001GB4297 20010926 (PCT/WO GB0104297)
Priority Application: GB 200023952 20000929
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 8489

English Abstract

French Abstract

Legal Status (Type, Date, Text)
Publication 20020404 A2 With declaration under Article 17(2)(a); without classification and without abstract; title not checked by the International Searching Authority.
Examination 20020822 Request for preliminary examination prior to end of 19th month from priority date
Fulltext Availability:
Claims

Claim
... the
resulting technical, workflow, and business knowledge.
The technology is underpinned by industry-specialist
knowledge **organised** by hot- **linked** workflow nodes that can
be viewed in either -a Project Management Stream, a Multi
Disciplinary...that define how a node relates to another
node. Nodes can be arranged in a **tree** structure wherein a
parent node can have a **number** of **child** **nodes** and these
nodes in turn can have **children** nodes. one particular **tree**
based structure is the so-called discipline structure,
where the project is broken down in...

32/5,K/13 (Item 13 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00883406 **Image available**
GLOBAL NETWORK COMPUTERS
ORDINATEURS DE RESEAU GLOBAL
Patent Applicant/Inventor:
ELLIS Frampton E III, Suite B-2, 2895 South Abingdon Street, Arlington, VA 22206-1331, US, US (Residence), US (Nationality)
Legal Representative:
LAZAR Dale S (et al) (agent), Pillsbury Winthrop LLP, 1600 Tysons Boulevard, McLean, VA 22102, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200217595 A2-A3 20020228 (WO 0217595)
Application: WO 2001US41849 20010823 (PCT/WO US0141849)
Priority Application: US 2000227660 20000825; US 2001308826 20010801
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H04L-029/06
International Patent Class: **G06F-001/00**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 29449

English Abstract
An apparatus for a network of computers is presented. A plurality of inner firewalls operate within a personal computer. The personal computer operates in a network of computers and includes at least one microprocessor and at least two memory components. The plurality of inner firewalls deny access to a first memory component of the personal computer by another computer through a network connection with the personal computer during a shared operation. The plurality of inner firewalls also allow access to a second memory component of the personal computer by the other computer through the network connection with the personal computer during the shared operation.

French Abstract
L'invention concerne un dispositif concu pour un reseau d'ordinateurs. Une pluralite de pare-feu interieurs est operationnelle a l'interieur d'un ordinateur personnel. Cet ordinateur personnel fonctionne dans un reseau d'ordinateurs et comprend au moins un microprocesseur et au moins deux elements de memoire. La pluralite de pare-feu interieurs empeche l'acces a un premier element de memoire de l'ordinateur personnel par un autre ordinateur par l'intermediaire d'une connexion reseau avec cet ordinateur personnel pendant une operation partagee. Cette pluralite de pare-feu interieurs permet egalement l'acces a un deuxieme element de memoire de l'ordinateur personnel par l'autre ordinateur pendant la connexion reseau avec cet ordinateur personnel pendant l'operation partagee.

Legal Status (Type, Date, Text)
Publication 20020228 A2 Without international search report and to be republished upon receipt of that report.
Examination 20020822 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20021003 Late publication of international search report
Republication 20021003 A3 With international search report.
Republication 20021003 A3 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

International Patent Class: **G06F-001/00**
Fulltext Availability:
Detailed Description

Detailed Description
... specifically, like the World Wide Web (WWW), or their equivalents or eventual successors like the **Grid** or MetaIntemet (and including Internet 11 and the Next Generation Internet, which are under development ...

...essentially all optical fiber transmission) with extremely broad bandwidth connections and virtually unlimited data transmission **speed** .

A prime characteristic of the Internet is the very large number of

communicating with the production flowline 40...

...The power fluid is thereby routed into the injection side of the dual function xmas **trees** via the injection choke valve 15. When leaving the downhole turbine 16, the power fluid...

...the produced hydrocarbons from the downhole separator 13 and brought to the wellhead (x-mas **tree** 1). From all producing wells the hydrocarbons are routed to the first header 6a via...

32/5,K/16 (Item 16 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00805406 **Image available**
DISTRIBUTED CACHE SYNCHRONIZATION PROTOCOL
PROTOCOLE DE SYNCHRONISATION D'ANTEMEMOIRE DISTRIBUEE
Patent Applicant/Assignee:
UTSTARCOM INC, 1275 Harbor Bay Parkway, Alameda, CA 94502, US, US (Residence), US (Nationality)
Inventor(s):
ZHANG Greg, 1321 Klamath Drive, San Jose, CA 95130, US,
Legal Representative:
BOYCE Justin (agent), Oppenheimer Wolff & Donnelly LLP, 1400 Page Mill Road, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200138983 A2-A3 20010531 (WO 0138983)
Application: WO 2000US32300 20001122 (PCT/WO US0032300)
Priority Application: US 99166882 19991122; US 2000210342 20000607
Designated States: CN
Main International Patent Class: G06F-011/00
International Patent Class: G06F-012/00; G06F-012/08; **G06F-013/14** ; G06F-015/00; G06F-015/16; G06F-015/17; G06F-015/163
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 27687

English Abstract
A process is provided for managing a distributed cache that stores cache information at a plurality of participating nodes of a network (100), the distributed cache including a plurality of cache entries each having an associated portion of the cache information, each of the participating nodes including an associated local memory storage system (131) for storing information including a local cache database (132) for storing locally owned ones of the cache entries. The process includes the steps of: performing topology discovery, maintenance, and hierarchy building sub-processes to establish a nodal hierarchy in the network in order to facilitate exchange of the cache entries between the participating nodes, the hierarchy being formed by a plurality of peer groups each including at least one associated member one of the participating nodes; and performing distributed cache synchronization (DCS) functions including copying and transferring selected ones of the cache entries to other ones of the participating nodes via the hierarchy in accordance with a DCS protocol.

French Abstract
L'invention concerne un procede permettant de gerer une antememoire

distribuee qui stocke des informations d'antememoire au niveau de plusieurs noeuds participants d'un reseau (100). L'antememoire distribuee comprend plusieurs entrees d'antememoire, chacune d'elles possedant une partie associees aux informations d'antememoire. Chaque noeud participant comprend un systeme de stockage de memoire (131) locale associee permettant de stocker des informations, notamment une base de donnees (132) d'antememoire locale destinee a stocker certaines des entrees d'antememoire localement possedees. Le procede consiste a executer des sous-procedes de decouverte de topologie, de maintenance, et de construction de hierarchie afin d'etablir une hierarchie nodale dans le reseau, et faciliter l'echange des entrees d'antememoire entre les noeuds participants, ladite hierarchie etant formee de plusieurs groupes pairs, chacun d'eux comprenant au moins un element associe aux noeuds participants; et a executer des fonctions de synchronisation d'antememoire distribuee (DCS), notamment des fonctions selectionnees de copie et de transfert des entrees d'antememoire vers les autres noeuds participants via la hierarchie en fonction du protocole DCS.

Legal Status (Type, Date, Text)
Publication 20010531 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010913 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20011004 Late publication of international search report
Republication 20011004 A3 With international search report.

...International Patent Class: **G06F-013/14**
Fulltext Availability:
Claims

Claim
... 413
/27
GLOBAUMIRRORED PROFILE
170 SUBSCRIBER LIST
164 /- 166 r 168 174
SUBSCRIBER BASE PROFILE **CONNECTIVITY**
KEY STATION POINTER INFORMATION
LOCATION
172
172
172
-y
FIG. 4C
/27
100
GROUP-1
LEVEL-1
/ 220
00 0...

...HELLO PARAMETER INFORMATION
PEER GROUP AGE COUNTER SEQUENCE NO.
MEMBER
y
FIG. 6D
270
NEIGHBOR **LIST**
NODE HOP **NUMBER**
(TTL RADIUS)
NODE -ID-1

NODE-ID-M
y
FIG. 6E
280 NODAL **HIERARCHY** **LIST** (FOR PHYSICAL NODE)
PEER-GROUP-ID
-PEER GROUP ID
PEER-GROUP-ID
PEER-GROUP-ID...NEW MOBILE HOST 1000
C@@ 1002
RECEIVE REGISTRATION MESSAGE FROM NEW HOST
SEARCH LOCAL PROFILE **LIST** USING RECEIVED **LINK** LAYER ID r
1006
OCIATED WITH r 1008
NEW HOST FOUNDIN YES Po PERFORM AUTHENTICATION...

...PROFILE
ASSOCIATED WITH NEW HOST
IS OWNED BY LOCAL BASE
STATION
1014
SEARCH MIRRORED PROFILE **LIST** USING **LINK** .a@E
R 71D
1016
10 8
OCIATED WITH NEW YE PERFORM AUTHENTICATION
HOST FOUND...

...NEW HOST
IS OWNED BY LOCAL BASE
STATION
FIG. 10A
/27
/ 1030
SEARCH GLOBAL SUBSCRIBER **LIST** USING r 1032
LINK LAYER ID
1042
1034 REQUEST COPY OF
T LISTE N G NO SUBSCRIBER PROFILE
S...

32/5,K/17 (Item 17 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00792496 **Image available**
METHOD AND ESTIMATOR FOR PROVIDING STORAGE MANAGEMENT
TECHNIQUE ET ESTIMATEUR POUR LA GESTION DES MOYENS DE STOCKAGE
Patent Applicant/Assignee:
ANDERSEN CONSULTING L L P, 100 South Wacker Drive, Chicago, IL 60603, US, US (Residence), US (Nationality)
Inventor(s):
MILLES Daniel, 8216 Cloverdale Lane, Rockford, IL 61107, US,
BOND William C, 21325 North White Pine, Kildeer, IL 60047, US,
Legal Representative:
RICHARDS Marc V (agent), Brinks Hofer Gilson & Lione, P.O. Box 10087, Chicago, IL 60610, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200126012 A1 20010412 (WO 0126012)
Application: WO 2000US27802 20001006 (PCT/WO US0027802)
Priority Application: US 99158259 19991006

Decisions regarding the type, quantity, **location** , and **connectivity** requirements for storage devices, and the resources needed to operate them, are based on business...

32/5,K/18 (Item 18 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00784184 **Image available**
A SYSTEM, METHOD FOR FIXED FORMAT STREAM COMMUNICATION IN A COMMUNICATION SERVICES PATTERNS ENVIRONMENT
SYSTEME, PROCEDE ET ARTICLE POUR FLUX DE FORMAT FIXE DANS UN ENVIRONNEMENT A CONFIGURATIONS DE SERVICES DE COMMUNICATION
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly LLP, P.O. Box 52037, Palo Alto, CA 94303-0746, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200117194 A2-A3 20010308 (WO 0117194)
Application: WO 2000US24114 20000831 (PCT/WO US0024114)
Priority Application: US 99386430 19990831
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DZ EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H04L-029/06
International Patent Class: G06F-017/22; H04L-029/12
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 149954

English Abstract
A system, method, and article of manufacture provide a fixed format stream-based communication system. A sending fixed format contract on interface code is defined for a sending system. A receiving fixed format contract on interface code is also defined for a receiving system. A message to be sent from the sending system to the receiving system is translated based on the sending fixed format contract. The message is then sent from the sending system and subsequently received by the receiving system. The message received by the receiving system is then translated based on the receiving fixed format contract.

French Abstract
L'invention concerne un systeme, un procede et un article pour systeme de communication a flux de format fixe. Un contrat de format fixe de transmission sur code d'interface est defini pour un systeme de transmission. Un contrat de format fixe de reception sur code d'interface est egalement defini pour un systeme de reception. Un message destine a

etre envoye du systeme de transmission au systeme de reception est converti sur la base du contrat de format fixe de transmission. Le message est ensuite transmis depuis le systeme de transmission, puis il est recu par le systeme de reception et converti sur la base du contrat de format fixe.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010816 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20020103 Late publication of international search report
Republication 20020103 A3 With international search report.
Fulltext Availability:
Claims

Claim
... report process is necessary, which results in improved performance.
Modules
Figure 32 shows the module **hierarchy** for the custom report process. The Figure shows the relationships between modules, not their associated... the application with conceptual integrity. That is, the logical Business Components serve as the direct **link** between the real-world busines(section) domain and the physical application. An important goal is...

32/5,K/19 (Item 19 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00784119
A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A REFRESHABLE PROXY POOL IN A COMMUNICATION ENVIRONMENT
SYSTEME, PROCEDE ET ARTICLE POUR GROUPE D'ELEMENTS MANDATAIRES (PROXY) RAFRAICHISSABLES DANS UN ENVIRONNEMENT A CONFIGURATIONS DE SERVICES DE COMMUNICATION
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918 , US,
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly LLP, 1400 Page Mill Road, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116668 A2-A3 20010308 (WO 0116668)
Application: WO 2000US24113 20000831 (PCT/WO US0024113)
Priority Application: US 99386239 19990831
Designated States: AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G06F-009/46
Publication Language: English
Filing Language: English

Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 149976

English Abstract
  A system, method, and article of manufacture are provided for interfacing a naming service and a client with the naming service allowing access to a plurality of different sets of services from a plurality of globally addressable interfaces. The naming service calls for receiving locations of the global addressable interfaces. As a result of the calls, proxies are generated based on the received locations of the global addressable interfaces. The proxies are received in an allocation queue where the proxies are then allocated in a proxy pool. Access to the proxies in the proxy pool is allowed for identifying the location of one of the global addressable interfaces in response to a request received from the client.

French Abstract
  L'invention concerne un systeme, un procede et un article permettant d'assurer l'interface entre un service de denomination et un client, le service de denomination donnant acces a plusieurs series de services a partir de plusieurs interfaces globalement adressables. Le service de denomination etablit des appels pour recevoir les emplacements des interfaces globalement adressables. Suite aux appels en question, les elements proxy sont etablis sur la base des emplacements recus pour les interfaces globalement adressables. Ces elements sont recus dans une file d'attente d'affectation puis attribues a un groupe d'elements proxy depuis la file d'attente. L'acces aux elements de ce groupe est autorise pour identifier l'emplacement de l'une des interfaces globalement adressables, en reponse a une demande recue de la part d'un client.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010809 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20020221 Late publication of international search report
Republication 20020221 A3 With international search report.

Fulltext Availability:
  Claims

Claim
... that are evaluated in this practice aid, all of them offer varying levels of mainframe **connectivity** . Does the client have existing personnel with mainframes - CICS experience? CICS/6000 has a programming ...60 percent of all new applications development will be based on assemblies of componentware, increasing **speed** to market and the ability to
cope with change (0.7 probability)."
Business Components and...

32/5,K/20 (Item 20 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00747364 **Image available**
NETWORK SWITCH FOR FAILURE RESTORATION
TRAITEMENT DE DEFAILLANCES DANS UN COMMUTATEUR DE RESEAU
Patent Applicant/Assignee:

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Inventor(s):
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Legal Representative:
TANG Henry, Baker Botts, LLP, 30 Rockefeller Plaza, New York, NY 10112-0228, US
Patent and Priority Information (Country, Number, Date):
Patent: WO 200060772 A1 20001012 (WO 0060772)
Application: WO 2000US8139 20000327 (PCT/WO US0008139)
Priority Application: US 99282609 19990401
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H04B-010/00
International Patent Class: H04B-010/08; H04B-010/12; H04B-010/20; H04B-017/00
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 14848

English Abstract
A system and method for automatically restoring a network which contains a node with a failed switch. Protection cycles are generated for the network to be restored and cyclegroups are generated from the protection cycles. Each node is provided with protection switches (105) which internally interconnect the input/output to connecting links via interconnecting protection fibers. The selection of which internal protection fibers upon which to switch transmitted information onto allows the node to be configured to create merged cyclegroups. Thus if a failure in the central switch is detected, the transmitted information is diverted to a selected protection fiber corresponding to a merged cycle group so that the information can be automatically passed around the failed switch via the protection fibers. Each protection switch has associated mapping data which defines which protection fiber will be switched to based upon the input and output link for the transmission that is required to be sent through the node. The system and method applies to non-planar networks as well as planar networks.

French Abstract
L'invention porte sur un systeme et un procede permettant de reconstituer automatiquement un reseau comprenant un noeud dont un commutateur est defaillant. Des cycles de protection sont generes pour la reconstitution du reseau et des groupes de cycles sont generes par les cycles de protection. Chaque noeud est muni de commutateurs de protection (105) qui connectent les ports d'entree et de sortie a des liaisons de connexion via des fibres de protection. La selection des fibres de protection internes par lesquelles les donnees transmises sont commutees permet au noeud de generer des groupes de cycles fusionnes. Ainsi, lorsqu'une defaillance est detectee dans le commutateur central, les donnees transmises sont deviees vers une fibre de protection correspondant a un groupe de cycles fusionne, de maniere a ce que les donnees puissent

...switch failure restoration method of the present invention applies to both planar and non-planar **topologies** . The methodology for non-planar restoration is also applicable to planar **topology** . In contrast to the planar case, where only one (priority) bi directional node-connection can...
...than one bi-directional node-connections that pass through a failed network switch. The actual **number** of **node** -connections that can be restored simultaneously depends upon the input- **link** , output- **link** pair of the **priority** node- **connection** as well as the rest of the node-connections passing through the failed switch. Restoration...the switch failure recovery
technique in accordance with the invention. Step 253 identifies the net **topology** as planar or non-planar using conventional techniques (e.g., the technique described above). Step...ASP3 and ASP4 are only used for switch failure restoration in networks with non-planar **topologies** . In networks with non-planar **topologies** , as soon as the protection switches are notified of the network switch failure by the...

32/5,K/21 (Item 21 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00533591 **Image available**
METHOD OF OPTIMIZING THE TOPOLOGY OF THE IEEE 1394 SERIAL BUS
PROCEDE D'OPTIMISATION DE LA TOPOLOGIE DU BUS SERIE IEEE 1394
Patent Applicant/Assignee:
SAMSUNG ELECTRONICS CO LTD,
CHEN Wei,
LEE Yun Gik,
Inventor(s):
CHEN Wei,
LEE Yun Gik,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9964943 A2 19991216
Application: WO 99KR291 19990612 (PCT/WO KR9900291)
Priority Application: KR 9821903 19980612
Designated States: CN JP US AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: G06F
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 1934

English Abstract
A method of optimizing the **topology** of the IEEE 1394 serial bus having a plurality of nodes each with communication ports, comprises the steps of **prioritizing** the nodes according to the **number** of the **ports** and the transmission **speed** , connecting a non-used port of the node of the first **priority** with a port of the node of the second priority, and repeating the previous step until all of the nodes are connected together, whereby the nodes are **connected** through the ports according to **priority** order.

French Abstract
Ce procede d'optimisation de la topologie du bus serie IEEE 1394 comprenant plusieurs noeuds, chacun dote de ports de communication, comprend les etapes consistant a classer par priorite les noeuds en

otaI **port number** of all of said nodes is equal to or greater than 2(N-1).

5...

32/5,K/22 (Item 22 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00406206 **Image available**
DEVICE FOR WORD PROCESSING
DISPOSITIF DE TRAITEMENT DE TEXTE
Patent Applicant/Assignee:
LENNERSTAD IDE,
LENNERSTAD Hakan,
Inventor(s):
LENNERSTAD Hakan,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9746951 A1 19971211
Application: WO 97SE984 19970604 (PCT/WO SE9700984)
Priority Application: SE 962215 19960604; SE 962990 19960816
Designated States: JP US AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: G06F-017/27
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 4065

English Abstract
A device for word processing is designed, when inputting characters, to automatically and in real time suggest a probable continuation of the formed combination of characters to a user. The word-processing device comprises an input unit (I), a first memory unit (M1) for storing of input characters, a display unit (D), a second memory unit (M2) and a comparator unit (C). When inputting a character in the first memory unit (M1), the comparator unit (C) compares the combination of characters created in the first memory unit (M1) with a word bank which is stored in the second memory unit (M2). The comparator unit (C) selects a word from the word bank, which is suggested to the user via the display unit (D). The comparator unit (C) is activatable to create or update, in the second memory unit (M2), the word bank based on the words in the first memory unit (M1), or in some other memory unit, whereupon the words in the second memory unit (M2) are sorted according to their priority value. The priority value of a word in the second memory unit (M2) is calculated on the basis of the number of presences of this word in the first memory unit (M1), or in some other memory unit.

French Abstract
L'invention concerne un dispositif de traitement de texte concu pour, lors de l'entree de caracteres, suggerer automatiquement et en temps reel a un utilisateur une suite probable de la combinaison de caracteres. Le dispositif de traitement de texte comporte une unite d'entree (I), une premiere memoire (M1) pour stocker les caracteres entres, et un affichage (D), une seconde memoire (M2) et un comparateur (C). Lors de l'entree d'un caractere dans la premiere memoire (M1), le comparateur (C) compare la combinaison de caracteres creee dans la premiere memoire a une banque de mots memorisee dans la seconde memoire (M2). Le comparateur (C) selectionne le mot dans la banque de mots qui est suggere par l'intermediaire de l'affichage (D). Le comparateur (C) est active pour

creer ou mettre a jour, dans le seconde memoire (M2), la banque de mots en fonction des mots dans la premiere memoire (M1), ou dans une autre memoire, apres quoi les mots dans la seconde memoire (M2) sont tries en fonction de leur valeur de priorite. La valeur de priorite d'un mot dans la seconde memoire (M2) est calculee en fonction du nombre d'apparition de celui-ci dans la premiere memoire (M1) ou dans un autre memoire.

Fulltext Availability:
Claims

Claim
... organised in a tree structure.

4 A device as claimed in claim 3, wherein said **tree** structure has a root, which branches off in a **number** of main **nodes** , each branching off in a number of subnodes, each in turn branching off in a...being designed to sort, in said update, the groups of data items according to said **priority** values and **connect** the groups of data items to the nodes, each group of data items being connected...in a tree structure.

10 A computer program as claimedoin claim 9, where in said **tree** structure has a root, which branches off in a **number** of main **nodes** , each branching off in a number of subnodes, each in turn branching off in a...

...being designed to sort, during said update, the groups of data items according to said **priority** values and **connect** the groups of data items to the nodes, each group of data items being connected...

32/5,K/23 (Item 23 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00362355 **Image available**
A METHOD AND APPARATUS FOR ROUTING MESSAGES IN A NETWORK OF NODES
PROCEDE ET DISPOSITIF D'ACHEMINEMENT DE MESSAGES DANS UN RESEAU DE NOEUDS
Patent Applicant/Assignee:
PHILIPS ELECTRONICS N V,
PHILIPS NORDEN AB,
Inventor(s):
DASGUPTA Aninda V,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9702680 A1 19970123
Application: WO 96IB613 19960627 (PCT/WO IB9600613)
Priority Application: US 95498715 19950630; US 95498286 19950630; US 95498285 19950630; US 95558447 19951116
Designated States: CN JP KR AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **H04L-012/28**
International Patent Class: H04L-12:56
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 10037

English Abstract

A system that includes a multihop broadcast network of nodes that may have a minimum of hardware resources, such as memory and processing power. The network is configured by gathering information concerning which nodes can communicate with each other using flooding with hop counts and parent routing protocols. A partitioned spanning tree is created and node identifiers are assigned so that the identifier of a child node includes as its most significant bits the identifier of its parent. This allows the identifier of the node to be used to determine if the node is to process or resend the packet so that the node can make complete packet routing decisions using only its own identifier.

French Abstract

On decrit un systeme presentant un reseau de noeuds de radiodiffusion a propagation par reflexions multiples, lequel peut comporter un minimum de ressources materielles, telles qu'une memoire et une puissance de traitement. Ce reseau est configure par collecte d'informations concernant ceux des noeuds qui peuvent communiquer les uns avec les autres selon une technique "d'arrosage" a l'aide de comptages de bonds et de protocoles d'acheminement de type principal/secondaire. Un arbre recouvrant subdivise est cree et des identificateurs de noeud sont assignes de maniere a ce que l'identificateur d'un noeud secondaire comprenne, en tant que bits les plus representatifs, l'identificateur de son noeud principal. Ceci permet a l'identificateur du noeud a utiliser de determiner si le noeud doit traiter ou renvoyer le paquet, de maniere a ce que le noeud puisse prendre des decision d'acheminement de paquets complets, a l'aide uniquement de son propre identificateur.

Main International Patent Class: **H04L-012/28**
Fulltext Availability:
Detailed Description

Detailed Description

... that results is like that of figure 2 and is represented in memory as a **linked list** such as illustrated in figures 15(a) and 15(b). Figure 15(a) depicts an...nodes as indicated by the graph connections. This arrangement is reflected in the pointer directed **linked list** data structure 310 of figure 15(b). As can be seen each item or entry...

...includes a physical ID field 314 containing the physical ID of the corresponding node, a **parent** ID field 316 that identifies the **parent node** , a hop **count** field 318 that includes the count of the 21 5 number of hops to the...

...in the NCN's memory. The spanning tree graph is built as a separated graph (**linked list** data structure) and the original graph is maintained for future network changes and additions. The...

...is provided herewith. The NCN 60 starts by considering itself the root of the spanning **tree** , and calculates its number of neighbors by adding one to the actual **number** of neighbor **nodes** in the graph. For example, NCN 60 has two neighbors so three is the calculated...

32/5,K/24 (Item 24 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00360258
ATM LOCAL ACCESS

ACCESS LOCAL MTA

Patent Applicant/Assignee:
GPT LIMITED,
ARNOLD John Spencer,
Inventor(s):
ARNOLD John Spencer,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9700583 A2 19970103
Application: WO 96GB1338 19960605 (PCT/WO GB9601338)
Priority Application: GB 9511844 19950610
Designated States: AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG US UZ VN KE LS MW SD SZ UG AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: H04Q-000/00
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 3503

English Abstract

In a Telecommunications Infrastructure an Access Network or Segment of an Access-Layer Infrastructure having a plurality of subscribers or extensions linked to one or more gateways having ports and providing access to/from higher network layers where the linking from the subscribers or extensions to the gateways is carried out by the statistical-multiplexing of ATM cells carried in time-slots formatted onto broadband bearers a desired gateway being identified by a number carried in the Virtual-Path Identifier field of each ATM cell and the source being identified by a number carried in an additional address field external to the ATM cell but internal to the time-slot, the linking from the gateways to the subscribers or extensions being by means of a distribution switch, the desired subscriber being identified by the number carried in the additional address field and the source being identified by the number carried in the Virtual Path Identifier field of the cell.

French Abstract

L'invention concerne une Infrastructure de Telecommunications, un Reseau d'Acces ou le Segment d'une Infrastructure a Acces par Couches ayant plusieurs abonnes ou plusieurs extensions relies a une ou plusieurs passerelles possedant des ports d'entree-sortie et fournissant l'acces vers/en provenance des couches plus hautes du reseau ou le raccordement partant des abonnes ou des extensions vers les passerelles est effectue par la multiplicite statistique des cellules MTA vehiculees dans des creneaux temporels formates sur des supports a large bande, ladite passerelle desiree etant identifiee par un nombre porte dans le Champ d'Identification Virtuel de chaque cellule MTA et la source etant identifiee par un nombre porte dans un champ d'adresses additionnel ne faisant pas partie de la cellule MTA mais faisant partie du creneau temporel, la liaison entre la passerelle et les abonnes ou les extensions se faisant par l'entremise d'un commutateur de distribution, l'abonne desire etant identifie par le nombre porte dans le champ d'adresses additionnel et la source etant identifiee par le nombre porte dans le Champ d'Identification Virtuel de la cellule.

Fulltext Availability:
Claims

Claim
... preceding claims in which the subscribers or extensions and the gateways are distributed across a **number** of **nodes** which are chain-linked by a slotted high-bandwidth bi-directional bearer forming a **topological** ring and where the device which links the chain across each node is a switch where through **connected** traffic has the first **priority** of access and where converging local traffic must wait in a first-in-first-out...

32/5,K/25 (Item 25 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00234265 **Image available**
SYSTEM FOR DIVIDING PROCESSING TASKS INTO SIGNAL PROCESSOR AND DECISION-MAKING MICROPROCESSOR INTERFACING
SYSTEME DE SEPARATION DES TACHES DE TRAITEMENT EN TACHES POUR INTERFACAGE AVEC UN PROCESSEUR DE SIGNAUX ET UN MICROPROCESSEUR DE PRISE DE DECISION
Patent Applicant/Assignee:
STAR SEMICONDUCTOR CORPORATION,
Inventor(s):
ROBINSON Jeffrey I,
ROUSE Keith,
KRASSOWSKI Andrew J,
MONTLICK Terry F,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9308524 A1 19930429
Application: WO 92US8954 19921014 (PCT/WO US9208954)
Priority Application: US 91776161 19911015
Designated States: AU CA JP KR AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE
Main International Patent Class: G06F-009/00
International Patent Class: G06F-09:40
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 219172

English Abstract
Architectures and methods are provided for efficiently dividing a processing task into tasks for a programmable real time signal processor (SPROC) (10) and tasks for a decision-making microprocessor (2120). The SPROC is provided with a non-interrupt structure where data flow is through a multiported central memory. The SPROC is also programmed in an environment which requires nothing more than graphic entry of a block diagram of the user's design. In automatically implementing the block diagram into silicon, the SPROC programming/development environment accounts for and provides software connection and interfaces with a host microprocessor (2120). The programming environment preferably includes: a high-level computer screen entry system which permits choosing, entry, parameterization, and connection of a plurality of functional blocks; a functional block cell library (2015) which provides source code representing the functional blocks; and a signal processor scheduler/compiler (2040) which uses the functional block cell library (2015) and the information entered into the high-level entry system to compile a program and to output source program code for a program memory and source data code for the data memory of the SPROC, as well as a symbol table which provides a memory map which maps SPROC addresses to

variable names which the microprocessor (2120) will refer to in separately compiling its program.

French Abstract

On decrit des architectures et procedes qui permettent de separer efficacement une tache de traitement en taches destinees a un processeur de signaux programmable fonctionnant en temps reel (SPROC)(10) et a un microprocesseur de prise de decision (2120). Le SPROC est dote d'une structure depourvue d'interruption ou le flux de donnees arrive par l'intermediaire d'une memoire centrale a ports multiples. Il est aussi programme dans un environnement n'exigeant rien d'autre que l'introduction graphique d'un schema global relatif aux intentions de l'utilisateur. Avec la realisation automatique du schema global dans le silicium, l'environnement de programmation et de developpement du SPROC prend en compte et fournit la connexion au logiciel et realise une interface avec un microprocesseur hote (2120). Cet environnement de programmation comporte de preference un systeme d'introduction a ecran d'affichage perfectionne qui permet de choisir, introduire, parametriser et fournit une connexion avec differents blocs fonctionnels; une bibliotheque a cellules de bloc fonctionnel (2015) qui fournit un code source representant les blocs fonctionnels; et un programmateur/compileur pour processeur de signal (2040). Ce dernier utilise la bibliotheque a cellules (2015) et l'information introduite dans le systeme d'introduction perfectionne pour compiler un programme et delivrer en sortie un code de programme source concernant une memoire du programme et un code de donnees source destine a la memoire de donnees du SPROC, ainsi qu'une table de symboles qu fournit une cartographie memorisee, contenant les adresses donnees par le SPROC aux differents noms auxquels le microprocesseur (2120) viendra se referer en compilant separement son propre programme.

Fulltext Availability:
Claims

Claim
... 192 to toggle to node 0 (operation), and switch 194 to toggle to an open **position** . Then the SPROC is ready to operate for its intended signal processing purposes. Although slave...

...ports 700 and data flow manager 600, is sent by the host 180 via host **port** 800 and the data RAM bus 125 as hereinafter described. As will be described hereinafter...

...host port 800. Serial data which is to be processed is sent into an input **port** 700 which is coupled to the data flow manager 600, which in turn forwards the data to appropriate **locations** (buffers) in the data RAM 100. In certain circumstances, described below, the DFM 600 will... embodiment hereof, access to the program RAM 150 by the GSPs 400 and the host **port** 800 and access **port** 900 is via time division multiplexing of a single input. Similarly, access to the data...running as hereinafter described), a pulse is sent to offset counter 656 which increases its **count** . In this manner the address output by adder 654 is changed to the next address...control the functioning of port 700 as one or the other. The serial data output **port** 700b seen in Fig. 5b is similar to the data input port 700a in many...twenty-four bit data word located at the data or program RAM address which was **placed** on the appropriate bus is read and latched either into the program data output register...filters. The filter design interface creates the custom code and definition data for filter cells **placed** in designs during diagram entry. The SPROCbuild utility converts signal flow block diagrams and their...maximum

32/5,K/26 (Item 26 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00180482 **Image available**
DISTRIBUTED INTELLIGENCE NETWORK USING TIME AND FREQUENCY MULTIPLEXING
RESEAU INFORMATIQUE DECENTRALISE A MULTIPLEXAGE TEMPOREL ET EN FREQUENCE
Patent Applicant/Assignee:
FIRST PACIFIC NETWORKS INC,
Inventor(s):
CHU Chi-Chi,
SANGAMESWARA Shanobhog,
VITA Peter Paul Lugtu,
OUYE Michael,
STEVENS David R F,
BARANSKI Celeste,
MONSSON Cai U,
MURPHY Timothy Patrick,
MURPHY Kevin Thomas,
SALDINGER Alan,
CRINGLE Robert J,
McNAMARA Robert P,
ELLIS Gary M,
GHATE Ranjit,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9013956 A1 19901115
Application: WO 89US1806 19890428 (PCT/WO US8901806)
Priority Application: WO 89US1806 19890428
Designated States: AT AU BE CH DE FR GB IT JP KR LU NL SE
Main International Patent Class: H04J-003/26
International Patent Class: H04J-04:00; H04J-03:06
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 72289

English Abstract
A distributed intelligence network (10) using time and frequency domain multiplexing. On power-up, each node (20) determines its skew and requests downloading of program code and configuration data. A node claims timeslots by transmitting a packet into an apparently empty timeslot and verifying receipt of its own packet.

French Abstract
Dans un reseau informatique decentralise a multiplexage temporel et en frequence, chaque noeud determine son obliquite lors de la mise sous tension et demande le telechargement du code de programmation et des donnees de configuration. Un noeud revendique une tranche de temps en transmettant un paquet a une tranche de temps apparemment vide et en verifiant si son propre paquet a ete recu.

Fulltext Availability:
Claims

Claim
... network 10 based on a bus medium 12. Bus medium 12 typically has the physical **topology** of a **tree** structure with a **number** of branches 121 to which various network nodes are coupled. The primary function of the...in a given node

is organized in a
layered structure based on the International Standards
Organization ("ISO") Open System **Interconnection**
Reference Model (110SI11). The OSI model contemplates an
organization having some or all of the...connection for a given PCM
Highway Receive timeslot. CPU 72 should not write to this
location during the **connection** , as doing this could corrupt
PCTL State Machine operation.
Bits Name Function
<4:0> PCM...connection for a given PCM
Highway Receive timeslot, CPU 72 should not write to this
location during the **connection** , as doing this could corrupt
PCTL State Machine operation.
Bits Name Function
<4:0> Network...

...a connection for a given PCM
Highway Transmit timeslot. Software should not write to this
location during the **connection** , as doing this could corrupt
PCTL State Machine operation.
Bits Name Function
<4:0> PCM...connection for a given PCM
Highway Transmit timeslot. CPU 72 should not write to this
location during the **connection** , as doing this could corrupt
PCTL State Machine operation.
Bits Name Function
<4:0> Network...will notify the same to the requesting
session entity6
3 2.2 Transport Interfaces
The **Interconnect** Voice Transport provides the above **listed** serv@
ices by a set of commands and Indications*
A requesting session entity will request...

32/5,K/27 (Item 27 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00157712 **Image available**
DRIVES WITH DOUBLE-ROTATING ELECTRIC MACHINES
MOTEURS AVEC MACHINES ELECTRIQUES A DOUBLE MOUVEMENT DE ROTATION
Patent Applicant/Assignee:
SCHUURSMA Johannes Karel,
Inventor(s):
SCHUURSMA Johannes Karel,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8904081 A1 19890505
Application: WO 88NL44 19881031 (PCT/WO NL8800044)
Priority Application: NL 872588 19871030
Designated States: AT AU BE CH DE DK FI FR GB HU IT JP KR LU NL SE SU US
Main International Patent Class: H02K-051/00
International Patent Class: H02K-07:10; H02K-16:00; F02N-11:04; F02N-05:04
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 10852

English Abstract
The double-rotating electric machine with its matching control-device

32/5,K/28 **(Item 28 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT

00146839
PROGRAMMABLE LOGIC CELL AND ARRAY
CELLULE LOGIQUE PROGRAMMABLE ET RESEAU
Patent Applicant/Assignee:
CONCURRENT LOGIC INC,
Inventor(s):
FURTEK Frederick C,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8803727 A1 19880519
Application: WO 87US2912 19871104 (PCT/WO US8702912)
Priority Application: US 86527 19861107
Designated States: AT AU BE CH DE FR GB IT JP KR LU NL SE
Main International Patent Class: H03K-019/177
International Patent Class: G06F-15:60
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 12754

English Abstract
Programmable logic cells, and arrays of those cells, having certain characteristics, including: (1) the ability to program each cell to act either as a logic element or as a logical identity element(s) between one or more inputs and one or more outputs; (2) the ability to rotate circuits by 90degrees and to reflect circuits about horizontal and vertical axes; (3) an integrated logic and communication structure which emphasizes strictly local communications; (4) simple logic functions available at the cell level, making available a very fine-grained logic structure; and (5) suitability for implementation of both synchronous and asynchronous logic, including **speed** -independent circuits. Cells are arranged in a **grid** , with each cell communicating with its north, east, west and south neighbors. The cells are programmable to several states. Using a graphics-based programming environment, the user may construct systems at a pictorial block diagram level, rather than having to be concerned about the detailed implementation of the internal structure of each block. Blocks may be rotated and they may be reflected about horizontal and vertical axes, to **place** their input and output **connections** on different sides and **positions** without altering the internal electrical operation of the blocks.

French Abstract
Des cellules logiques programmables ainsi que des reseaux de ces cellules presentent certaines caracteristiques et notamment: (1) la capacite de programmer chaque cellule afin qu'elle agisse soit comme element logique soit comme element(s) d'identite logique entre une ou plusieurs entrees et une ou plusieurs sorties; (2) la capacite d'imprimer une rotation de 90degrees a des circuits et de reflechir des circuits autour d'axes horizontaux et verticaux; (3) une structure integree logique et de communication qui met l'accent strictement sur les communications locales; (4) des fonctions logiques simples disponibles au niveau de la cellule, mettant a disposition une structure logique serree; et (5) l'aptitude a la mise en oeuvre de circuits logiques a la fois synchrones et asynchrones, y compris des circuits independants de la vitesse. Ces cellules sont agencees en reseau, chaque cellule

communiquant avec ses voisines du nord, de l'est, de l'ouest et du sud. Les cellules sont programmables sur plusieurs etats. A l'aide d'un environnement de programmation base sur des graphiques, l'utilisateur peut elaborer des systemes au niveau de l'organigramme illustre, plutot que d'avoir a se preoccuper de la mise en oeuvre detaillee de la structure interne de chaque case. Des cases peuvent subir une rotation et elles peuvent etre reflechies autour d'axes horizontaux et verticaux, afin de placer leurs connexions d'entree et de sortie sur des cotes et positions differents sans modifier le fonctionnement electrique interne des cases.

English Abstract

...grained logic structure; and (5) suitability for implementation of both synchronous and asynchronous logic, including **speed** -independent circuits. Cells are arranged in a **grid** , with each cell communicating with its north, east, west and south neighbors. The cells are...

...Blocks may be rotated and they may be reflected about horizontal and vertical axes, to **place** their input and output **connections** on different sides and **positions** without altering the internal electrical operation of the blocks.

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File 347:JAPIO Oct 1976-2003/Feb(Updated 030603)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200338
         (c) 2003  Thomson Derwent
? ds

Set     Items   Description
S1     163894   TREE OR TREES OR HIERARCH? OR TREEMAP? OR GRID OR GRIDS OR
             TOPOLOG?????? ? OR PYRAMID? ? OR CASCAD? OR SUBTREE? ?
S2      88362   PARENT? ? OR CHILD OR CHILDREN
S3     983418   SPEED OR SPEEDS
S4       4304   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (PORT OR PORTS)
S5       2953   (NUMBER OR QUANTITY? OR QUANTITIES OR COUNT OR COUNTS)(2N)-
             (NODE OR NODES)
S6      55875   PRIORIT? OR RANK???? ?
S7      61153   SORT OR SORTS OR SORTED OR SORTING?
S8      56188   ORGANIS? OR ORGANIZ?
S9    3989281   PLACE? ? OR PLACING? OR PLACEMENT? OR PLACED OR POSITION???
              ? OR LOCAT???? ? OR LIST OR LISTS OR LISTED OR LISTING? ? OR
             SITUATE? ? OR SITUATING OR SITED
S10    246400   S3:S5 AND S6:S9
S11      3102   S10 AND S1:S2
S12    153501   S6:S9(5N)(CONNECT? OR INTERCONNECT? OR LINK??? ? OR INTERL-
             INK?)
S13       158   S11 AND S12
S14      6081   S3:S5(S)S1:S2
S15        73   S14 AND S12
S16      3726   S3:S5(S)S12
S17        66   S16 AND S1:S2
S18    163738   S3:S5(S)S6:S9
S19      1636   S18 AND S1:S2
S20        82   S19 AND S12
S21      8820   IC='G06F-000':IC='G06F-000/01'
S22     65301   IC='G06F-001':IC='G06F-001/016'
S23      8488   IC='G06F-013/14'
S24     44475   IC='H04L-012/28':IC='H04L-012/2856'
S25      1102   MC='T01-C07D'
S26       158   S13 OR S15 OR S17 OR S20
S27         2   S26 AND S21:S23
S28         9   S26 AND S24
S29       162   S25 AND S3:S5
S30        25   S29 AND S6:S9
S31    976736   IC='G06F'
S32        49   S31 AND S26
S33    319443   IC='H04L'
S34         9   S32 AND S33
S35        39   S27:S28 OR S30 OR S34
S36        39   IDPAT (sorted in duplicate/non-duplicate order)
S37        38   IDPAT (primary/non-duplicate records only)
? t37/9/all

 37/9/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003  Thomson Derwent. All rts. reserv.

014997627    **Image available**
WPI Acc No: 2003-058142/200305
XRPX Acc No: N03-045158
  PCI bus bridging method for high  speed  data transfer, involves avoiding
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execution of posted memory writes and requests of main request queue, if one posted memory write exists in retry list

Patent Assignee: JAIN S (JAIN-I); LACKEY S A (LACK-I)
Inventor: JAIN S; LACKEY S A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020144039	A1	20021003	US 2001823205	A	20010330	200305	B

Priority Applications (No Type Date): US 2001823205 A 20010330
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020144039	A1		9	G06F-012/00	

Abstract (Basic): US 20020144039 A1

NOVELTY - Posted memory writes (PWMs) and requests not allowed to execute before a prior PWM are stored in a main request queue (MRQ). Requests allowed to execute before a prior PWM are stored in a special mode request queue (SMRQ). Destination bus control is arbitrated among the queues and a retry **list** which stores the requests from the queues, such that if a PWM is in the **list** , then the contents of MRQ are not executed.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for bus bridging apparatus.

USE - For bridging peripheral component interface (PCI) buses or PCI-X bus with other buses for high **speed** data transfer.

ADVANTAGE - The method of arbitrating destination bus control, avoids execution of contents of the MRQ if a PWM exists in the retry **list** , thereby eliminating the ordering rule violation.

DESCRIPTION OF DRAWING(S) - The figure shows a simple representation of the bus bridging process.

pp; 9 DwgNo 1/4

Title Terms: BUS; BRIDGE; METHOD; HIGH; **SPEED** ; DATA; TRANSFER; AVOID; EXECUTE; POST; MEMORY; WRITING; REQUEST; MAIN; REQUEST; QUEUE; ONE; POST; MEMORY; WRITING; EXIST; RETRY; **LIST**
Derwent Class: T01
International Patent Class (Main): G06F-012/00
International Patent Class (Additional): G06F-013/14; G06F-013/38
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-H05B2

37/9/2 (Item 2 from file: 350)

014965204 **Image available**
WPI Acc No: 2003-025718/200302
XRPX Acc No: N03-020742

Transmission control protocol connection control method in internet, involves searching connection condition control table with connection **pointer** list **acquired with respect to expanded offset**

Patent Assignee: NIPPON DENKI SOFTWARE KK (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002330161	A	20021115	JP 2001135830	A	20010507	200302	B

Priority Applications (No Type Date): JP 2001135830 A 20010507
Patent Details:

Patent No Kind Lan Pg   Main IPC   Filing Notes
JP 2002330161 A   7 H04L-012/56

Abstract (Basic): JP 2002330161 A
NOVELTY - A base table is generated during the initial stage starting of a connection control program. A TCP connection is carried out based on the offset of the entry of pointer **list** groups of the **tree** structure in the base table. A connection condition control table is searched based on the **connection** pointer **list** formed with respect to expanded offset.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for TCP connection control device.
USE - Transmission control protocol (TCP) connection control method in internet.
ADVANTAGE - Enables accessing a TCP connection at high **speed** without increasing average access time proportionally with respect to number of registered connections.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the TCP connection control device. (Drawing includes non-English language text).
pp; 7 DwgNo 1/3
Title Terms: TRANSMISSION; CONTROL; PROTOCOL; CONNECT; CONTROL; METHOD; SEARCH; CONNECT; CONDITION; CONTROL; TABLE; CONNECT; POINT; **LIST** ; ACQUIRE; RESPECT; EXPAND; OFFSET
Derwent Class: T01; W01
International Patent Class (Main): **H04L**-012/56
International Patent Class (Additional): **G06F-009/445** ; **G06F-013/00** ; **G06F-015/00** ; **G06F-017/30**
File Segment: EPI
Manual Codes (EPI/S-X): T01-F01B; T01-F05B; T01-H; T01-J; T01-J05B; W01-A03B; W01-A06G2

37/9/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014423364 **Image available**
WPI Acc No: 2002-244067/200230
XRPX Acc No: N02-188893
Network topology detection method for network of electronic devices, involves resolving positions **of end stations initially and subsequently resolving topology of remaining devices in network**
Patent Assignee: 3COM CORP (THRE-N)
Inventor: LINZELL C R; VALENTINE S P; WALKER L A
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2362060	A	20011107	GB 20009045	A	20000412	200230	B
GB 2362060	B	20020424	GB 20009045	A	20000412	200235	

Priority Applications (No Type Date): GB 20009045 A 20000412
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2362060	A		12	H04L-012/56	
GB 2362060	B			H04L-012/56	

Abstract (Basic): GB 2362060 A
NOVELTY - The **positions** of the end stations are resolved initially by determining the ports of each managed device connected to

the end station. The topology of the remaining devices is resolved subsequently.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for computer program storing network topology detecting instructions.

USE - For discovering network topology for networks e.g. Ethernet, wide area network (WAN), local area network (LAN) of electronic devices e.g. workstations, personal computers, servers, hubs, routers, bridges, switches, etc.

ADVANTAGE - **Speed** of the process is improved by reducing the number of interrogations efficiently.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the network topology detection process.

pp; 12 DwgNo 3/3

Title Terms: NETWORK; TOPOLOGICAL; DETECT; METHOD; NETWORK; ELECTRONIC; DEVICE; RESOLUTION; **POSITION** ; END; STATION; INITIAL; SUBSEQUENT; RESOLUTION; TOPOLOGICAL; REMAINING; DEVICE; NETWORK

Derwent Class: T01; W01

International Patent Class (Main): H04L-012/56

File Segment: EPI

Manual Codes (EPI/S-X): **T01-C07D** ; T01-N02A2; T01-N02A3B; T01-N02A3C; T01-S03; W01-A06E; W01-A06F1C; W01-A06X

37/9/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014050678 **Image available**

WPI Acc No: 2001-534891/200159

XRPX Acc No: N01-397087

Task suspension and resumption in multitasking host adapter, involves executing single instruction in on-chip sequencer to suspend main routine execution in bus interface

Patent Assignee: ADAPTEC INC (ADAP-N)

Inventor: YOUNG B A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6253272	B1	20010626	US 9888810	A	19980602	200159	B

Priority Applications (No Type Date): US 9888810 A 19980602

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6253272	B1		14	G06F-013/14	

Abstract (Basic): US 6253272 B1

NOVELTY - A single instruction is executed in an on-chip sequencer (230) by writing return address for main routine in related memory **location** , to suspend execution of main routine. The main routine used by input-output bus interface (210) is branched to subroutine. Another instruction is executed to restore return address in memory so that subroutine is returned to main routine and sequencer resumes execution of main routine in that address.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the input-output bus interface integrated circuit.

USE - For task suspension and resumption in multitasking host adapters used for interfacing between input-output buses like host bus, SCSI bus. The host adapters can be utilized with new high **speed** technologies for data storage such as fiber channel that require multitasking.

ADVANTAGE - The use of single instructions in the two routines, eliminates many lines of existing firmware instruction which in turn reduces the silicon area require to store the firmware. Hence enhances execution performance.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of interface integrated circuit for input-output bus.

Input-output bus interface (210)

On-chip sequencer (230)

pp; 14 DwgNo 2B/5

Title Terms: TASK; SUSPENSION; RESUME; HOST; EXECUTE; SINGLE; INSTRUCTION; CHIP; SEQUENCE; SUSPENSION; MAIN; ROUTINE; EXECUTE; BUS; INTERFACE

Derwent Class: T01

International Patent Class (Main): G06F-013/14

File Segment: EPI

Manual Codes (EPI/S-X): T01-C07C; **T01-C07D** ; T01-F02A; T01-F03A; T01-F04; T01-F05A; T01-H01A; T01-H05B1; T01-H05B2; T01-M02C1

37/9/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014011917

WPI Acc No: 2001-496131/200154

Related WPI Acc No: 2001-136291

XRPX Acc No: N01-367628

Power consumption reducing method for computer system buses, involves placing bus node in low power state, returning it to fully powered state on bus transaction request

Patent Assignee: INTEL CORP (ITLC)

Inventor: CRUZ C A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6282665	B1	20010828	US 971816	A	19971231	200154	B
			US 2000519131	A	20000306		

Priority Applications (No Type Date): US 971816 A 19971231; US 2000519131 A 20000306

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6282665	B1		15	G06F-001/26	Cont of application US 971816 Cont of patent US 6131167

Abstract (Basic): US 6282665 B1

NOVELTY - The power management circuit **places** a bus node in a reduced power consumption state. A multiport bus interface provided by a link circuit coupled to a physical layer (PHY), forwards messages received when the bus in the reduced power mode. The node is returned to the full power state when a wake-up event occurs.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) A bus power management circuit.

(2) A bus circuit with a physical layer to provide access to a bus to capture events from the bus.

USE - The power management method is applicable to systems in which the power consumption of a node's bus interface is controlled independently from the power state of the rest of the bus node. This is suitable for situations such as battery powered notebook computers.

ADVANTAGE - The method is used to reduce the power consumed by a bus node (claimed). It can be used in buses that need non-interruptible

signaling capability such that reducing the power consumption on a node does not interfere with normal signaling on the bus (claimed).

pp; 15 DwgNo 0/7

Technology Focus:

TECHNOLOGY FOCUS - INDUSTRIAL STANDARDS - The method of bus power management complies to IEEE 1394-1995 for high **speed** serial buses.

Title Terms: POWER; CONSUME; REDUCE; METHOD; COMPUTER; SYSTEM; BUS; **PLACE** ; BUS; NODE; LOW; POWER; STATE; RETURN; POWER; STATE; BUS; TRANSACTION; REQUEST

Derwent Class: T01

International Patent Class (Main): G06F-001/26

File Segment: EPI

Manual Codes (EPI/S-X): **T01-C07D** ; T01-F05B3; T01-H05B3; T01-H07A1; T01-H07A2; T01-H07B; T01-H07P; T01-L01

37/9/6 (Item 6 from file: 350)

013964120 **Image available**

WPI Acc No: 2001-448334/200148

XRPX Acc No: N01-331979

Private network information management system for ATM switching system, displays call connection path diagram along with call details, when call is connected through private networknetwork interface

Patent Assignee: NIPPON DENKI TSUSHIN SYSTEM KK (NIDE)

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001156789	A	20010608	JP 99332913	A	19991124	200148	B
JP 3382906	B2	20030304	JP 99332913	A	19991124	200324	

Priority Applications (No Type Date): JP 99332913 A 19991124

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001156789	A		24	H04L-012/28	
JP 3382906	B2		23	H04L-012/28	Previous Publ. patent JP 2001156789

Abstract (Basic): JP 2001156789 A

NOVELTY - A network management device designates generated call identifiers to every call connected through private network:network interface (PNNI) between ATM switching systems (1-30 - 1-35) based on call control, network **topology** , call arrival probability, link and call detailed information acquired from respective databases. A production unit produces call connection path diagram which is displayed with call details to user.

DETAILED DESCRIPTION - A call identifier generation unit generates call identifier which identifies call connected through private network:network interface (PNNI) provided between asynchronous transfer mode (ATM) switching systems. The arriving calls are arranged in the order of **priority** and a designated transit **list** path (DTL), is generated for call connection. A notification unit indicates the network management device about network **topology** information consisting of DTL, call control information, arrival probability information, link state information and call detail information which are acquired from respective databases. Using all information, the network management device outputs call connection path. A call path diagram production unit generates call connection path diagram which is displayed along with call details.

USE - For asynchronous transfer mode (ATM) switching system in which call is connected through private network:network interface (PNNI).

ADVANTAGE - Using call identifier, call connected is easily identified in real time at high **speed** . Also, connection path established is easily understood by call **connection** path diagram. Since designated transit **list** path of present call **connection** path and past call connection path is stored in memory, the connection established is easily identified.

DESCRIPTION OF DRAWING(S) - The figure shows the component block diagram of network information management system. (Drawing includes non-English language text).

ATM switching systems (1-30 - 1-35)

pp; 24 DwgNo 1/19

Title Terms: PRIVATE; NETWORK; INFORMATION; MANAGEMENT; SYSTEM; ATM; SWITCH ; SYSTEM; DISPLAY; CALL; CONNECT; PATH; DIAGRAM; CALL; DETAIL; CALL; CONNECT; THROUGH; PRIVATE; NETWORK; NETWORK; INTERFACE

Derwent Class: W01

International Patent Class (Main): **H04L-012/28**

International Patent Class (Additional): H04L-012/24; H04L-012/26; H04M-003/00

File Segment: EPI

Manual Codes (EPI/S-X): W01-A03B1

37/9/7 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013714789 **Image available**

WPI Acc No: 2001-199013/200120

XRPX Acc No: N01-142861

Hierarchical **-structure determination method for computer network peripheral device connection, involves removing loop which neither transmits nor receives request marker, in** tree **-like** topology **of connected network**

Patent Assignee: HEWLETT-PACKARD CO (HEWP)

Inventor: LE T V

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001024684	A	20010126	JP 2000176197	A	20000613	200120	B
US 6496485	B1	20021217	US 99332796	A	19990614	200307	

Priority Applications (No Type Date): US 99332796 A 19990614

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001024684	A		7	H04L-012/44	
US 6496485	B1			H04L-012/413	

Abstract (Basic): JP 2001024684 A

NOVELTY - Each connected node of **tree** structure has an unique **priority** number. The **priority number** of **connected nodes** are compared. The adjacent nodes other than higher **priority** node transmits request marker to higher **priority** node. The loop in which request marker is neither transmitted nor received, is removed from the **tree** -like **topology** .

USE - For determining **hierarchical** -structure for connecting computer network and peripheral device

DESCRIPTION OF DRAWING(S) - The figure shows the explanatory diagram of **hierarchical** -structure determination method.

pp; 7 DwgNo 4/4
Title Terms: **HIERARCHY** ; STRUCTURE; DETERMINE; METHOD; COMPUTER; NETWORK; PERIPHERAL; DEVICE; CONNECT; REMOVE; LOOP; NEITHER; TRANSMIT; NOR; RECEIVE; REQUEST; MARK; **TREE** ; **TOPOLOGICAL** ; CONNECT; NETWORK
Derwent Class: T01; W01
International Patent Class (Main): **H04L-012/413** ; **H04L-012/44**
International Patent Class (Additional): **G06F-013/38** ; **H04L-012/28**
File Segment: EPI
Manual Codes (EPI/S-X): T01-H07C; W01-A06E2A

37/9/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013130879 **Image available**
WPI Acc No: 2000-302750/200026
XRPX Acc No: N00-226252
Drive circuit slew rate controller couples selected and enabled predrivers and output drivers having same slew rate
Patent Assignee: RAMBUS INC (RAMB-N)
Inventor: CHAN Y; HO T; LAU B C; PATEL S A; WEI J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6047346	A	20000404	US 9817529	A	19980202	200026	B

Priority Applications (No Type Date): US 9817529 A 19980202
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6047346	A		19	G06F-013/14	

Abstract (Basic): US 6047346 A

NOVELTY - Several predriver groups are coupled to corresponding selector circuits comprising NAND gates (752,753). The output of predrivers are coupled to the input of corresponding output drivers in one shot pulse (713). The selected and enabled output drivers and predrivers having the same slew rate are coupled together.

DETAILED DESCRIPTION - The NAND gates (752,753) coupled to multiplexers are used as selector circuits and NMOS transistors are used as output drivers. The selector circuits have data inputs and clock inputs. The clock input selects the data inputs which inturn enable one or more of the output drivers. The slew rate is determined by varying the number of predrivers and output drivers that are enabled. The slew rate is increased by increasing the number of predrivers coupled to the corresponding input of output drivers. INDEPENDENT CLAIMS are also included for the following:

(a) interface circuit;

(b) drive circuit slew rate adjusting method

USE - Drive circuit for increasing transmission rates between controller circuit and memory.

ADVANTAGE - Since slew rate of output signal is controlled using a slew rate control circuit, data transfer takes **place** at high **speed** . The high **speed** communications reduces delays during processor access of external memory, thus increasing processors performance.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of slew rate controller.

One shot pulse (713)

NAND gates (752,753)

pp; 19 DwgNo 7/11

Title Terms: DRIVE; CIRCUIT; SLEW; RATE; CONTROL; COUPLE; SELECT; ENABLE; OUTPUT; DRIVE; SLEW; RATE
Derwent Class: T01
International Patent Class (Main): G06F-013/14
File Segment: EPI
Manual Codes (EPI/S-X): T01-C07C; **T01-C07D** ; T01-L09

37/9/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013099792 **Image available**
WPI Acc No: 2000-271664/200023
XRPX Acc No: N00-203404

Co-axial connector arrangement for transmitting signals between circuit boards, includes conductive barrier partially surrounding elongated pin, with connector coupled to one bias voltage line

Patent Assignee: INTEL CORP (ITLC); INTLE CORP (INTL-N)
Inventor: TURNER L O
Number of Countries: 086 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200016444	A1	20000323	WO 99US20551	A	19990907	200023	B
AU 9958157	A	20000403	AU 9958157	A	19990907	200034	
US 6183266	B1	20010206	US 98151394	A	19980910	200109	

Priority Applications (No Type Date): US 98151394 A 19980910
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200016444	A1	E	25	H01R-009/09	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW

AU 9958157	A	H01R-009/09	Based on patent WO 200016444
US 6183266	B1	H01R-012/00	

Abstract (Basic): WO 200016444 A1

NOVELTY - An elongated pin (110) and socket (115) removably engaging elongated pin mounted on circuit boards (160,170), respectively, are electrically connected to signal lines (165,175) of their respective circuit boards. A conductive barrier partially surrounding the elongated pin, has a connector coupled to one bias voltage line.

DETAILED DESCRIPTION - The socket has an insulating material disposed between the barrier and socket portion. The barrier is **positioned** at a preset distance. An INDEPENDENT CLAIM is also included for the method of mounting coaxial connectors.

USE - For transmitting signals between circuit boards in communication system for high **speed** signaling.

ADVANTAGE - High **speed** signal transmission is realized by providing barrier which has stacking connector that is connected to bias voltage signal line. The connector provides propagation of high frequency signal between circuit boards thus reducing noise and impedance.

DESCRIPTION OF DRAWING(S) - The figure shows the coaxial connector providing electrical contact between circuit boards.

Conductive base (105)

Elongated pin (110)
Socket (115)
Circuit boards (160,170)
Bias voltage line (182)
pp; 25 DwgNo 1/7
Title Terms: CO; AXIS; CONNECT; ARRANGE; TRANSMIT; SIGNAL; CIRCUIT; BOARD; CONDUCTING; BARRIER; SURROUND; ELONGATE; PIN; CONNECT; COUPLE; ONE; BIAS; VOLTAGE; LINE
Derwent Class: T01; V04; W01
International Patent Class (Main): H01R-009/09; H01R-012/00
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; V04-B01; V04-B03; V04-M01; V04-M05; V04-M30G; W01-A07H1

37/9/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013025884 **Image available**
WPI Acc No: 2000-197735/200018
Related WPI Acc No: 2000-197705; 2000-197728; 2000-197734
XRPX Acc No: N00-146605

Primary and secondary bus architecture for computer system e.g. graphics system in which primary to secondary bus interface modules interconnect the primary and secondary buses

Patent Assignee: PIXELFUSION LTD (PIXE-N)
Inventor: PHELPS R C; WINSER P A
Number of Countries: 090 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2341772	A	20000322	GB 9820430	A	19980918	200018	B
WO 200017759	A2	20000330	WO 99GB3089	A	19990916	200024	
AU 9958777	A	20000410	AU 9958777	A	19990916	200035	
EP 1112539	A2	20010704	EP 99946365	A	19990916	200138	
			WO 99GB3089	A	19990916		

Priority Applications (No Type Date): GB 9820430 A 19980918; GB 9820410 A 19980918; GB 9820412 A 19980918; GB 9820428 A 19980918
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2341772	A		56	G06F-013/40	
WO 200017759	A2	E		G06F-013/00	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW

AU 9958777	A		G06F-013/00	Based on patent WO 200017759
EP 1112539	A2	E	G06F-013/00	Based on patent WO 200017759

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Abstract (Basic): GB 2341772 A
NOVELTY - The bus architecture comprises of a primary bus (3) connected to latency intolerant modules and a secondary bus (4) connected to latency tolerant modules. The primary to secondary bus interface modules (5) interconnect the primary and secondary buses.
USE - Computer system e.g. graphics system, personal computer, laptop, microcomputer, microprocessor, simultaneous instruction

multiple data (SIMD) applications, parallel processing, set-top boxes or consumer appliances.

ADVANTAGE - The architecture is flexible enough to cope with the differing needs that individual modules will **place** on the system. Allows efficient high **speed** and high volume data transfer between modules of the system.

DESCRIPTION OF DRAWING(S) - The drawing shows a architecture for use in computer system.

Primary bus (3)

Secondary bus (4)

Primary to secondary bus interface modules (5)

pp; 56 DwgNo 2/31

Title Terms: PRIMARY; SECONDARY; BUS; ARCHITECTURE; COMPUTER; SYSTEM; GRAPHIC; SYSTEM; PRIMARY; SECONDARY; BUS; INTERFACE; MODULE; INTERCONNECT ; PRIMARY; SECONDARY; BUS

Derwent Class: T01; W01; W04

International Patent Class (Main): G06F-013/00; G06F-013/40

International Patent Class (Additional): G06F-013/364; H04L-012/40; H04L-012/403

File Segment: EPI

Manual Codes (EPI/S-X): **T01-C07D** ; T01-H05B3; T01-H07A; T01-P02A; W01-A06B1; W01-A06B5A; W01-A06E2A; W01-A06G3; W04-X02C

37/9/11 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013025880 **Image available**

WPI Acc No: 2000-197731/200018

XRPX Acc No: N00-146601

Bus arbitration unit for computer systems e.g. computer games consoles in which the transaction request is selected from filtered requests

Patent Assignee: PIXELFUSION LTD (PIXE-N)

Inventor: PHELPS R C; WINSER P A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2341768	A	20000322	GB 9820419	A	19980918	200018	B

Priority Applications (No Type Date): GB 9820419 A 19980918

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2341768	A		51	H04L-012/403	

Abstract (Basic): GB 2341768 A

NOVELTY - The bus architecture is connected to modules and consists of a filter for filtering the transaction requests from the modules to retain the request from modules with highest **priority** level. Transaction request is selected from filtered requests (27) for sending a request grant message to module from which the selected transaction was received.

DETAILED DESCRIPTION - The apparatus includes a levels assenter for assigning a predetermined number of **priority** levels for each module, a queue assignor for assigning each module an initial **position** within a stack or queue (26) and a receiver (25) for receiving respective transaction request from the modules.

USE - Computer system e.g. graphics system, personal computer, laptop, microcomputer, microprocessor, simultaneous instruction multiple data (SIMD) applications, parallel processing, set-top boxes,

computer game console or consumer appliances.
ADVANTAGE - The architecture is flexible enough to cope with the differing needs that individual modules will **place** on the system. Allows efficient high **speed** and high volume data transfer between modules of the system.
DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of the arbitration unit.
Transaction request receiver (25)
Queue (26)
Filtered requests (27)
pp; 51 DwgNo 12/31

Title Terms: BUS; ARBITER; UNIT; COMPUTER; SYSTEM; COMPUTER; GAME; CONSOLE; TRANSACTION; REQUEST; SELECT; FILTER; REQUEST
Derwent Class: T01; W01; W04
International Patent Class (Main): H04L-012/403
International Patent Class (Additional): G06F-013/364; G06F-013/40; H04L-012/40
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-H05B3; T01-H07A; T01-P02A; W01-A03A ; W01-A06B1; W01-A06B5A; W01-A06E2A; W01-A06F; W04-X02C

37/9/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013025879 **Image available**
WPI Acc No: 2000-197730/200018
XRPX Acc No: N00-146600

Bus arbitration for computer system e.g. computer game console has bus architecture with separate read, write and transactions on the buses control

Patent Assignee: PIXELFUSION LTD (PIXE-N)
Inventor: PHELPS R C; WINSER P A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2341767	A	20000322	GB 9820415	A	19980918	200018	B

Priority Applications (No Type Date): GB 9820415 A 19980918
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2341767	A		50	H04L-012/403	

Abstract (Basic): GB 2341767 A
NOVELTY - The bus architecture is connected to modules and has separate read, write and transactions on the buses control. The first arbiter (32) controls initiating transactions i.e. use of write and transaction buses and the second arbiter (33) controls the return transactions i.e. use of read bus on the bus architecture.
USE - Computer system e.g. graphics system, personal computer, laptop, microcomputer, microprocessor, simultaneous instruction multiple data (SIMD) applications, parallel processing, set-top boxes, computer game console or consumer appliances.
ADVANTAGE - The architecture is flexible enough to cope with the differing needs that individual modules will **place** on the system. Allows efficient high **speed** and high volume data transfer between modules of the system.
DESCRIPTION OF DRAWING(S) - The drawing shows a arbitration unit.
First arbiter (32)

Second arbiter (33)
pp; 50 DwgNo 20/31
Title Terms: BUS; ARBITER; COMPUTER; SYSTEM; COMPUTER; GAME; CONSOLE; BUS; ARCHITECTURE; SEPARATE; READ; WRITING; TRANSACTION; BUS; CONTROL
Derwent Class: T01; W01; W04
International Patent Class (Main): H04L-012/403
International Patent Class (Additional): G06F-013/364; G06F-013/40; H04L-012/40
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-H05B3; T01-H07A2; T01-P02A; W01-A03A; W01-A06B1; W01-A06B5A; W01-A06E2A; W01-A06F; W04-X02C

37/9/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013025878 **Image available**
WPI Acc No: 2000-197729/200018
XRPX Acc No: N00-146599
Bus architecture for computer system e.g. computer game console has physically separated write and read data bus
Patent Assignee: PIXELFUSION LTD (PIXE-N)
Inventor: PHELPS R C; WINSER P A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2341766	A	20000322	GB 9820413	A	19980918	200018	B

Priority Applications (No Type Date): GB 9820413 A 19980918
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2341766	A		52	H04L-012/40	

Abstract (Basic): GB 2341766 A
NOVELTY - The bus architecture (12,13,14) is connected to module (10,11) and consists of physically separated write data bus (13) and read data bus (14) for transferring data between the module. The transaction bus is also connected to the bus architecture for transferring control data between nodules.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM includes a method of retrieving data in a computer system.
USE - Computer system e.g. graphics system, personal computer, laptop, microcomputer, microprocessor, simultaneous instruction multiple data (SIMD) applications, parallel processing, set-top boxes, computer game console or consumer appliances.
ADVANTAGE - The architecture is flexible enough to cope with the differing needs that individual modules will **place** on the system. Allows efficient high **speed** and high volume data transfer between modules of the system.
DESCRIPTION OF DRAWING(S) - The drawing shows the bus architecture.
Module (10,11)
Bus architecture (12,13,14)
Write data bus (13)
Read data bus (14)
pp; 52 DwgNo 5/31
Title Terms: BUS; ARCHITECTURE; COMPUTER; SYSTEM; COMPUTER; GAME; CONSOLE; PHYSICAL; SEPARATE; WRITING; READ; DATA; BUS
Derwent Class: T01; W01; W04
International Patent Class (Main): H04L-012/40
International Patent Class (Additional): G06F-013/362; G06F-013/40;

H04L-012/403
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-H05B3; T01-H07A2; T01-P02A; W01-A06B1; W01-A06B5A; W01-A06E2A; W04-X02C

37/9/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013025877 **Image available**
WPI Acc No: 2000-197728/200018
Related WPI Acc No: 2000-197705; 2000-197734; 2000-197735
XRPX Acc No: N00-146598

Arbitration unit for granting access to the bus in a computer system e.g. graphic system in which modules issues empty packets during periods when the bus is idle

Patent Assignee: PIXELFUSION LTD (PIXE-N)
Inventor: PHELPS R C; WINSER P A
Number of Countries: 090 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2341765	A	20000322	GB 9820412	A	19980918	200018	B
WO 200017759	A2	20000330	WO 99GB3089	A	19990916	200024	
AU 9958777	A	20000410	AU 9958777	A	19990916	200035	
EP 1112539	A2	20010704	EP 99946365	A	19990916	200138	
			WO 99GB3089	A	19990916		

Priority Applications (No Type Date): GB 9820412 A 19980918; GB 9820410 A 19980918; GB 9820428 A 19980918; GB 9820430 A 19980918
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2341765	A		51	H04L-012/403	
WO 200017759	A2	E		G06F-013/00	
	Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW				
	Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW				
AU 9958777	A			G06F-013/00	Based on patent WO 200017759
EP 1112539	A2	E		G06F-013/00	Based on patent WO 200017759
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				

Abstract (Basic): GB 2341765 A

NOVELTY - The arbitration unit (21) for granting access to the bus in response to requests received from the modules (M1-M5) issues empty packets during periods when the bus is idle. The empty packets are used by the module to gain access to by the bus without making a specific request to the arbitration unit for a dedicated packet. The unit is connected to the modules, which are connected to the bus architecture (20).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM includes a method of granting bus access to a module in a computer system.

USE - Computer system e.g. graphics system, personal computer, laptop, microcomputer, microprocessor, simultaneous instruction multiple data (SIMD) applications, parallel processing, set-top boxes, computer game console or consumer appliances.

ADVANTAGE - The architecture is flexible enough to cope with the differing needs that individual modules will **place** on the system.

Allows efficient high **speed** and high volume data transfer between modules of the system.

DESCRIPTION OF DRAWING(S) - The drawing shows the apparatus incorporating an arbitration unit.

Arbitration unit (21)

Modules (M1-M5)

Bus architecture (20)

pp; 51 DwgNo 11/31

Title Terms: ARBITER; UNIT; ACCESS; BUS; COMPUTER; SYSTEM; GRAPHIC; SYSTEM; MODULE; ISSUE; EMPTY; PACKET; PERIOD; BUS; IDLE

Derwent Class: T01; W01; W04

International Patent Class (Main): G06F-013/00; H04L-012/403

International Patent Class (Additional): G06F-013/362

File Segment: EPI

Manual Codes (EPI/S-X): **T01-C07D** ; T01-H05B3; T01-H07A; T01-P02A; W01-A03A ; W01-A03B; W01-A06B1; W01-A06B5A; W01-A06E2A; W01-A06F; W01-A06G2; W04-X02C

37/9/15 (Item 15 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013009831 **Image available**

WPI Acc No: 2000-181683/200016

XRPX Acc No: N00-134100

Networking switch with network presence of a bridge used in interconnected computer networks

Patent Assignee: SHANI R (SHAN-I)

Inventor: SHANI R

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6023563	A	20000208	US 96700017	A	19960820	200016	B

Priority Applications (No Type Date): US 96700017 A 19960820

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6023563	A		17	G06F-013/14	

Abstract (Basic): US 6023563 A

NOVELTY - The networking switch (3,4,5) has a packet transmitter that selectively sends data packets to a destination address stored a database, and forwards data packets, having destination address not registered in the database, to a router (2). The packet transmitter receives a response from the router, and learns the destination address from the received response.

DETAILED DESCRIPTION - The network switch also has a network **topology** learner that gathers network **topology** data contained in the message traffic, and correlates station MAC addresses with station network addresses. The database stores the **topology** data. A data packet modifier changes the address data contained in the data packets. The network switch is used for interconnected computer networks, in which each network has stations with MAC addresses and network addresses and handles message traffic in the form of data packets in accordance with a set of inter-network protocols using a network addressing scheme.

INDEPENDENT CLAIMS are also included for the following:

(a) the configuration operation method of the interconnected networks;

(b) and the operation method of the interconnected networks.

USE - Used in interconnected computer networks. For **connecting** a computer station **located** on one network to another station or stations **located** on another network.

ADVANTAGE - Transfers data between stations **located** in different networks to relieve workload on the router. Features silicon-based design, thereby, processing, modifying, transmitting and filtering frames at wire **speed** . Saves cost of routers and improves existing slow processing time. Can be installed without altering the network operation, and without being registered as an additional router device but acts in a silent, unobtrusive manner within the network. Capable of processing inter-network communications wherein two stations connect to the network switch through the same port and use different network or subnet numbers.

DESCRIPTION OF DRAWING(S) - The figure shows a typical network made up of computer stations, repeaters, bridges and routers.

Router (2)

Networking switch (3,4,5)

pp; 17 DwgNo 3/6

Title Terms: SWITCH; NETWORK; PRESENCE; BRIDGE; INTERCONNECT; COMPUTER; NETWORK

Derwent Class: T01

International Patent Class (Main): **G06F-013/14**

File Segment: EPI

Manual Codes (EPI/S-X): T01-H05B2; T01-H07C5A; T01-H07P

37/9/16 (Item 16 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012934072 **Image available**

WPI Acc No: 2000-105919/200009

XRPX Acc No: N00-081331

Topology **optimization method for IEEE 1394 serial bus of multimedia instruments e.g. HDTV, DVD, DVC**

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)

Inventor: CHEN W; LEE Y G; JIN W; LEE Y J

Number of Countries: 022 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9964943	A2	19991216	WO 99KR291	A	19990612	200009	B
EP 1027640	A2	20000816	EP 99925442	A	19990612	200040	
			WO 99KR291	A	19990612		
KR 2000001563	A	20000115	KR 9821903	A	19980612	200059	
CN 1273652	A	20001115	CN 99800897	A	19990612	200115	
KR 298979	B	20010906	KR 9821903	A	19980612	200227	
JP 2002517967	W	20020618	WO 99KR291	A	19990612	200242	
			JP 2000553880	A	19990612		
JP 3295074	B2	20020624	WO 99KR291	A	19990612	200243	
			JP 2000553880	A	19990612		

Priority Applications (No Type Date): KR 9821903 A 19980612

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9964943	A2	E	23	G06F-000/00	
Designated States (National): CN JP US					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1027640	A2	E		G06F-001/00	Based on patent WO 9964943
Designated States (Regional): DE GB					
KR 2000001563	A			H04L-012/28	

CN 1273652	A		G06F-013/14	
KR 298979	B		G11B-020/10	Previous Publ. patent KR 2000001563
JP 2002517967	W	25	H04L-012/28	Based on patent WO 9964943
JP 3295074	B2	7	H04L-012/28	Previous Publ. patent JP 200217967 Based on patent WO 9964943

Abstract (Basic): WO 9964943 A2

NOVELTY - The serial bus comprises multiple nodes, each with communication ports and **priority** is assigned to nodes according to their count and transmission **speed** . Then unused port in node of first **priority** is **connected** to port in node of second **priority** and this process is continued until all nodes are connected.

DETAILED DESCRIPTION - The total **port number** of **nodes** is compared with reference value which varies with **number** of **nodes** , to determine whether or condition for **topology** optimization is satisfied. **Priority** is assigned to nodes only if the condition is satisfied.

USE - For IEEE 1394 serial bus used in multimedia instruments such as HDTV, DVD, DVC.

ADVANTAGE - Enables construction of **topology** which increases **speed** capacity of each node in bus.

DESCRIPTION OF DRAWING(S) - The figure shows the flow chart illustrating **topology** optimization method.

pp; 23 DwgNo 2/4

Title Terms: **TOPOLOGICAL** ; OPTIMUM; METHOD; SERIAL; BUS; INSTRUMENT; HDTV

Derwent Class: T01

International Patent Class (Main): **G06F-000/00** ; **G06F-001/00** ; **G06F-013/14** ; G11B-020/10; **H04L-012/28**

International Patent Class (Additional): **G06F-013/00** ; **G06F-013/18** ; **G06F-013/20** ; **G06F-013/26** ; **G06F-013/28** ; **G06F-013/30** ; **G06F-013/36** ; **G06F-013/38** ; **H04L-012/44**

File Segment: EPI

Manual Codes (EPI/S-X): T01-C07C5; **T01-C07D** ; T01-J30

37/9/17 (Item 17 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012445122 **Image available**

WPI Acc No: 1999-251230/199921

XRPX Acc No: N99-187840

Topology **correction system for restarting communication from condition communication becomes impossible** - has adjacent communication node which **is determined connectable to transmission line without forming logic loop when logical** connection **is confirmed in** location **after notice of** connection **is transmitted**

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11074889	A	19990316	JP 97231940	A	19970828	199921	B

Priority Applications (No Type Date): JP 97231940 A 19970828

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11074889	A		14	H04L-012/28	

Abstract (Basic): JP 11074889 A

NOVELTY - An adjacent communication node is determined connectable

to a transmission line without forming a logic loop when a logical **connection** is confirmed in a **location** , in which adjacent communication node is determined whether it is connectable, after a notice of connection is transmitted to the communication node. INDUSTRIAL STANDARD - The system uses an interface such as a high-**speed** serial bus with Institute of Electronics and Electrical Engineers (IEEE) 1394 specification.

USE - For restarting communication from condition communication becomes impossible.

ADVANTAGE - Makes communication possible when logic loop of serial bus is accidentally formed. DESCRIPTION OF DRAWING(S) - The figure shows a flowchart for explaining the **topology** correction system.

Dwg.1/13

Title Terms: **TOPOLOGICAL** ; CORRECT; SYSTEM; RESTART; COMMUNICATE; CONDITION; COMMUNICATE; IMPOSSIBLE; ADJACENT; COMMUNICATE; NODE; DETERMINE; CONNECT; TRANSMISSION; LINE; FORMING; LOGIC; LOOP; LOGIC; CONNECT; **LOCATE** ; AFTER; NOTICE; CONNECT; TRANSMIT

Derwent Class: W01

International Patent Class (Main): **H04L-012/28**

International Patent Class (Additional): H04L-012/40; H04L-012/42

File Segment: EPI

Manual Codes (EPI/S-X): W01-A06A1; W01-A06B1; W01-A06B2; W01-A06B5

37/9/18 (Item 18 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011783012 **Image available**

WPI Acc No: 1998-199922/199818

XRPX Acc No: N98-158973

Photoelectric compound home network system - has interface units individually provided at terminal devices respectively connected to photoelectric compound outlets to which several domestic locations **are** connected **in star** topology

Patent Assignee: SHARP KK (SHAF)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10051464	A	19980220	JP 96205530	A	19960805	199818	B

Priority Applications (No Type Date): JP 96205530 A 19960805

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10051464	A		12	H04L-012/28	

Abstract (Basic): JP 10051464 A

The system includes photoelectric compound outlets (11) provided with an optical fibre for data transmission and a power line in on body. An electronic data distribution panel (13) **connects** several domestic **locations** in star **topology** to the photoelectric compound outlets.

A data generation unit generates data related to terminal devices (12) respectively connected to the photoelectric compound outlets. Interface units (15) each having a memory that stores address data, are individually provided at the terminals devices.

USE - For batching of power supply and data transmitted to e.g. telephone, CATV, TV.

ADVANTAGE - Eliminates complication of address setting of user since it enables automatic assignment of terminal address to each

domestic **location** . Enables **priority** processing to terminal e.g. telephone that needs real time processing. Need to construct large extension of input-output terminal, fibre optic, and photoelectric compound outlet for electronic data distribution panel becomes unnecessary. Performs high- **speed** data communication.

Dwg.1/12

Title Terms: PHOTOELECTRIC; COMPOUND; HOME; NETWORK; SYSTEM; INTERFACE; UNIT; INDIVIDUAL; TERMINAL; DEVICE; RESPECTIVE; CONNECT; PHOTOELECTRIC; COMPOUND; OUTLET; DOMESTIC; **LOCATE** ; CONNECT; STAR; **TOPOLOGICAL**
Index Terms/Additional Words: **COMMUNITY** ; **ANTENNA** ; TELEVISION
Derwent Class: W01; W02
International Patent Class (Main): **H04L-012/28**
International Patent Class (Additional): **G06F-013/00** ; H04B-003/54; H04B-010/00; H04B-010/12; H04B-010/13; H04B-010/135; H04B-010/14; H04B-010/22
File Segment: EPI
Manual Codes (EPI/S-X): W01-A06B5; W01-A06B7; W01-A06C1; W02-F03A3

37/9/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011682817 **Image available**
WPI Acc No: 1998-099726/199809
XRPX Acc No: N98-079913

Real-time multi-tasking device with multiple application interface - includes high performance microprocessor and special designed hardware modules

Patent Assignee: DEFENCE DEPT CHUNG SHAN INST (DEFE-N)
Inventor: DING K; LII S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 318912	A	19971101	TW 96109785	A	19960813	199809	B

Priority Applications (No Type Date): TW 96109785 A 19960813
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 318912	A		31	G06F-003/00	

Abstract (Basic): TW 318912 A

The device connects different external peripherals and processes each peripheral data in real time. It includes a high performance microprocessor and special designed hardware modules. The microprocessor has embedded real-time software with multi-tasking feature. The software builds a platform which allows both periodical and aperiodical application tasks running on it simultaneously. Tasks are **prioritized** and scheduled to execute in a pre-defined order and are completed within a tolerable time limit.

USE - For controlling military or industrial equipments in time critical environment.

ADVANTAGE - Possible to connect high **speed** and low **speed** peripherals.

Dwg.11/11

Title Terms: REAL; TIME; MULTI; DEVICE; MULTIPLE; APPLY; INTERFACE; HIGH; PERFORMANCE; MICROPROCESSOR; SPECIAL; DESIGN; HARDWARE; MODULE
Derwent Class: T01
International Patent Class (Main): G06F-003/00
File Segment: EPI

Manual Codes (EPI/S-X): **T01-C07D**

37/9/20 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011638699 **Image available**
WPI Acc No: 1998-055607/199806
Related WPI Acc No: 1991-001384; 1993-368174
XRPX Acc No: N98-044110
Spanning tree organisation **for high-** speed **mesh** connected **network - has point-to-point links, cut-through, non-blocking switching and provides automatic reconfiguration of spanning** tree **for route control**
Patent Assignee: DIGITAL EQUIP CORP (DIGI)
Inventor: BIRRELL A D; MURRAY H G; NEEDHAM R M; RODEHEFFER T L; SATTERTHWAITE E H; SCHROEDER M D; THACKER C P
Number of Countries: 004 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 817424	A2	19980107	EP 90305289	A	19900516	199806 B
			EP 97201068	A	19900516	

Priority Applications (No Type Date): US 89370285 A 19890622
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 817424	A2	E	66	H04L-012/28	Div ex application EP 90305289
					Div ex patent EP 404337

Designated States (Regional): DE FR GB IT

Abstract (Basic): EP 817424 A
The high- **speed** data transport network is formed as a mesh of high- **speed** , point-to-point links. Each switch uses cut-through packet transfer to reduce latency. The nodes define links as uplinks or downlinks with all uplinks leading to the root of a spanning **tree** . Many data packets move through the network concurrently and each moves via uplinks toward their target and never use an uplink after using a downlink.
When a change in the network arises, each switch automatically detects the change, e.g. additions or failures. All of the switches participate in a distributed reconfiguration process that rapidly re-establishes legal routes. Any change in the configuration of the network causes the switches to redetermine their relative **tree positions** in the spanning **tree** .
ADVANTAGE - Provides very-high aggregate bandwidth, broadcast features, fast automatic reconfiguration and low latency.
Dwg.20/20
Title Terms: SPAN; **TREE** ; **ORGANISE** ; HIGH; **SPEED** ; MESH; CONNECT; NETWORK; POINT; POINT; LINK; CUT; THROUGH; NON; BLOCK; SWITCH; AUTOMATIC; RECONFIGURE; SPAN; **TREE** ; ROUTE; CONTROL
Derwent Class: T01; W01
International Patent Class (Main): **H04L-012/28**
File Segment: EPI
Manual Codes (EPI/S-X): T01-H07C5; T01-M02A1; W01-A03B; W01-A06B4; W01-A06B5A; W01-A06E1; W01-A06G2; W01-A06G3

37/9/21 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011627375 **Image available**
WPI Acc No: 1998-044503/199805
XRPX Acc No: N98-035553

Computer system with multiple zoom port interface - has two or more connectors used for receiving devices selected by user and buffer circuitry for selectively enabling one of devices to access feature bus

Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: BOESCH S C; JUENGER R E
Number of Countries: 020 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 814401	A2	19971229	EP 97304063	A	19970611	199805	B
JP 10143651	A	19980529	JP 97157157	A	19970613	199832	
US 5841994	A	19981124	US 96663957	A	19960614	199903	

Priority Applications (No Type Date): US 96663957 A 19960614
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 814401	A2	E	10	G06F-003/14	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 10143651	A		10	G06T-001/60	
US 5841994	A			G06F-013/00	

Abstract (Basic): EP 814401 A

The computer includes a processor, a frame buffer memory (50), while a graphics controller (48) is coupled to the processor and the frame buffer memory. The graphics controller includes a feature bus for allowing a device external to the graphics controller to store data in the frame buffer memory. Two or more connectors are used for receiving devices selected by the user. A buffer circuitry (26) for selectively enabling one of the devices to access the feature bus. The two or more connectors includes at least one personal computer card slot assembly.

The two or more connectors include a docking station (38) connector. Logic circuitry is provided for controlling the buffer circuitry that includes storage **locations** for one or more control signals, while the processor is arranged for executing code for controlling the buffer circuitry.

USE/ADVANTAGE - In computer with **number** of zoom **port** interfaces. Allows multiple slots for receiving zoom video devices without conflicts occurring on feature bus and computer is compatible with docking station, which may need connection to feature bus.

Dwg.2/6

Title Terms: COMPUTER; SYSTEM; MULTIPLE; ZOOM; PORT; INTERFACE; TWO; MORE; CONNECT; RECEIVE; DEVICE; SELECT; USER; BUFFER; CIRCUIT; SELECT; ENABLE; ONE; DEVICE; ACCESS; FEATURE; BUS
Derwent Class: T01
International Patent Class (Main): G06F-003/14; G06F-013/00; G06T-001/60
International Patent Class (Additional): G06F-003/00; G06F-003/153
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-M06A1B

37/9/22 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011484259 **Image available**
WPI Acc No: 1997-462164/199743

XRPX Acc No: N97-384873
Bus interface appts - has signal path switching functional board which is connected to rear side of back plane of rack at position where load wiring plate is attached
Patent Assignee: NIPPON TELEGRAPH & TELEPHONE CORP (NITE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9212267	A	19970815	JP 9619588	A	19960206	199743	B

Priority Applications (No Type Date): JP 9619588 A 19960206
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9212267	A		4	G06F-003/00	

Abstract (Basic): JP 9212267 A

The appts has a rack whose back plane comprises signal wirings (3A,3B). Multiple load wiring plates (4-1 - 4-m) are connected to the back plane through a set of respective connectors. A signal path switching board (7) is connected to the rear side of the back plane at a **position** where the load wiring plate is connected.

A receiving element (12) which receives the signal is provided in the load wiring plate. A driver element (11) which transmits the signal is also mounted on the load wiring plate. The switching board has a transmission delay adjustment part (9) and a switch (8) that connects signal wiring to load wiring part.

ADVANTAGE - Improves signal transmission **speed** . Decreases number of signal wiring for load wiring plate.

Dwg.3/5

Title Terms: BUS; INTERFACE; APPARATUS; SIGNAL; PATH; SWITCH; FUNCTION; BOARD; CONNECT; REAR; SIDE; BACK; PLANE; RACK; **POSITION** ; LOAD; WIRE; PLATE; ATTACH
Derwent Class: T01
International Patent Class (Main): G06F-003/00
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-L02C

37/9/23 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011294387 **Image available**
WPI Acc No: 1997-272292/199724
XRPX Acc No: N97-225593
Multiprocessor computer system with shared virtual maintenance channel - has flow controlled virtual channel with buffers for each physical communication link storing packets with data transferred between processors, non flow controlled channel has maintenance channel buffers similarly assigned
Patent Assignee: CRAY RES INC (CRAY)
Inventor: THORSON G M
Number of Countries: 021 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9716792	A1	19970509	WO 96US15117	A	19960923	199724	B
EP 858633	A1	19980819	EP 96932293	A	19960923	199837	
			WO 96US15117	A	19960923		
EP 858633	B1	19991124	EP 96932293	A	19960923	199954	
			WO 96US15117	A	19960923		

DE 69605319	E	19991230	DE 605319	A	19960923	200007
			EP 96932293	A	19960923	
			WO 96US15117	A	19960923	
US 6055618	A	20000425	US 95550992	A	19951031	200027
JP 2000508094	W	20000627	WO 96US15117	A	19960923	200036
			JP 97517327	A	19960923	

Priority Applications (No Type Date): US 95550992 A 19951031
Cited Patents: 1.Jnl.Ref; EP 479520; US 4330858; US 4630259; US 4933933
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9716792	A1	E	33	G06F-015/163	
Designated States (National): CA JP					
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 858633	A1	E		G06F-015/163	Based on patent WO 9716792
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
EP 858633	B1	E		G06F-015/163	Based on patent WO 9716792
Designated States (Regional): DE FR GB					
DE 69605319	E			G06F-015/163	Based on patent EP 858633
					Based on patent WO 9716792
US 6055618	A			G06F-015/16	
JP 2000508094	W		34	G06F-015/177	Based on patent WO 9716792

Abstract (Basic): WO 9716792 A

The computer system includes several processors and physical communication links interconnecting them in an n-dimensional **topology** . A flow controlled virtual channel (50 to 56) has virtual channel buffers assigned to each physical communication link to store packets containing normal traffic information to be transferred between the processors.

A non flow controlled virtual maintenance channel has maintenance channel buffers assigned to each link to store packets of maintenance information to be transferred between the processors. The maintenance channel is assigned a higher **priority** for accessing the **links** than the flow controlled virtual channel. The non flow controlled channel is accessible through system software running on the multiprocessor system from any processor.

USE - Relates to field of high **speed** digital data processing systems and to multiprocessor computer system with virtual maintainance channel sharing same physical communication links with other virtual routing channels.

ADVANTAGE - Read write registers can be written to and read from through non flow controlled virtual maintenance channel to verify that certain routes are valid.

Dwg.5/7

Title Terms: MULTIPROCESSOR; COMPUTER; SYSTEM; SHARE; VIRTUAL; MAINTAIN; CHANNEL; FLOW; CONTROL; VIRTUAL; CHANNEL; BUFFER; PHYSICAL; COMMUNICATE; LINK; STORAGE; PACKET; DATA; TRANSFER; PROCESSOR; NON; FLOW; CONTROL; CHANNEL; MAINTAIN; CHANNEL; BUFFER; SIMILAR; ASSIGN
Derwent Class: T01
International Patent Class (Main): **G06F-015/16** ; **G06F-015/163** ; **G06F-015/177**
International Patent Class (Additional): **H04L-012/00**
File Segment: EPI
Manual Codes (EPI/S-X): T01-H07C5A; T01-M02

37/9/24 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011154928 **Image available**
WPI Acc No: 1997-132852/199712
XRPX Acc No: N97-109633

Multiple level minimum logic network - in which switching control is distributed throughout multiple nodes in structure, such that supervisory controller providing global control function and complex logic is avoided

Patent Assignee: REED C S (REED-I); US NAT SECURITY AGENCY (USGO)
Inventor: REED C S
Number of Countries: 070 Number of Patents: 020
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9704399	A2	19970206	WO 96US11828	A	19960719	199712	B
AU 9664988	A	19970218	AU 9664988	A	19960719	199723	
WO 9704399	A3	19970410				199729	
EP 842473	A2	19980520	EP 96924569	A	19960719	199824	
			WO 96US11828	A	19960719		
US 5996020	A	19991130	US 95505513	A	19950721	200003	
JP 2000500253	W	20000111	WO 96US11828	A	19960719	200013	
			JP 97506822	A	19960719		
MX 9800626	A1	19981101	MX 98626	A	19980121	200022	
KR 99035759	A	19990525	WO 96US11828	A	19960719	200032	
			KR 98700415	A	19980120		
NZ 313016	A	20000526	NZ 313016	A	19960719	200033	
			WO 96US11828	A	19960719		
AU 725826	B	20001019	AU 9664988	A	19960719	200057	
EP 1058194	A2	20001206	EP 96924569	A	19960719	200064	
			EP 2000120146	A	19960719		
EP 1058195	A2	20001206	EP 96924569	A	19960719	200064	
			EP 2000120188	A	19960719		
AU 200056520	A	20001123	AU 9664988	A	19960719	200067	N
			AU 200056520	A	20000906		
US 6272141	B1	20010807	US 95505513	A	19950721	200147	
			US 99397333	A	19990914		
US 20010021192	A1	20010913	US 95505513	A	19950721	200155	
			US 99397333	A	19990914		
			US 2001852009	A	20010507		
US 20010034798	A1	20011025	US 95505513	A	19950721	200170	
			US 99397333	A	19990914		
			US 2001850953	A	20010507		
ES 2160556	T1	20011116	EP 2000120188	A	19960719	200201	
NZ 503094	A	20011130	NZ 313016	A	19960719	200207	
			NZ 503094	A	19960719		
MX 204102	B	20010906	MX 98626	A	19980121	200239	
CA 2227271	C	20021231	CA 2227271	A	19960719	200307	
			WO 96US11828	A	19960719		

Priority Applications (No Type Date): US 95505513 A 19950721; AU 200056520 A 20000906; US 99397333 A 19990914; US 2001852009 A 20010507; US 2001850953 A 20010507
Cited Patents: 7.Jnl.Ref; WO 9412939; WO 9516240; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9704399	A2	E	90	G06F-015/16	
Designated States (National): AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TT UA UG UZ VN					
Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG					
AU 9664988	A				Based on patent WO 9704399
EP 842473	A2	E		G06F-015/173	Based on patent WO 9704399

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI NL PT SE

US	5996020	A		G06F-013/00	
JP	2000500253	W	152	G06F-015/173	Based on patent WO 9704399
MX	9800626	A1		G06F-015/16	
KR	99035759	A		G06F-015/16	Based on patent WO 9704399
NZ	313016	A		G06F-015/173	Based on patent WO 9704399
AU	725826	B		G06F-015/16	Previous Publ. patent AU 9664988 Based on patent WO 9704399
EP	1058194	A2 E		G06F-015/80	Div ex application EP 96924569 Div ex patent EP 842473

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI NL PT SE

EP	1058195	A2 E		G06F-015/80	Div ex application EP 96924569 Div ex patent EP 842473

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI NL PT SE

AU	200056520	A		H04L-012/54	Div ex application AU 9664988 Div ex patent AU 725826
US	6272141	B1		H04L-012/28	Div ex application US 95505513 Div ex patent US 5996020
US	20010021192	A1		H04L-012/28	Div ex application US 95505513 Div ex application US 99397333 Div ex patent US 5996020
US	20010034798	A1		H04L-012/28	Div ex application US 95505513 Div ex application US 99397333 Div ex patent US 5996020 Div ex patent US 6272141
ES	2160556	T1		G06F-015/80	Based on patent EP 1058195
NZ	503094	A		H04L-012/58	Div ex application NZ 313016 Div ex patent NZ 313016
MX	204102	B		G06F-015/16	
CA	2227271	C	E	G06F-015/173	Based on patent WO 9704399

Abstract (Basic): WO 9704399 A

The network structure uses a data flow technique that is based on timing and **positioning** of messages communicating through the **interconnect** structure, and includes a number of interconnect lines selectively connecting the nodes in a multiple level structure in which the levels include a richly interconnected collection of rings.

The multiple level structure includes a number of J+1 levels in a **hierarchy** of levels, and a number of 2(to power J)K nodes ate each level. If integer K is an odd **number** , the **nodes** on level M are **situated** on 2(to power J-M) rings, with each ring including 2(to power M)K nodes. Message data leaves the interconnect structure from nodes on a level zero. Each node has multiple communication terminals, some of which are data input and output terminals, and others are control input and output terminals.

USE - Multiple level minimum logic network interconnect structure for computing and communication systems, with very high bandwidth and low latency, for use as interconnect structure for massively parallel computer, e.g supercomputer, or for linking group of workstations, computers, terminals, ATM machines, elements of national flight control systems etc.

ADVANTAGE - Eliminates global control function and avoids complex logic structures.

Dwg.1a/25

Title Terms: MULTIPLE; LEVEL; MINIMUM; LOGIC; NETWORK; SWITCH; CONTROL; DISTRIBUTE; MULTIPLE; NODE; STRUCTURE; SUPERVISION; CONTROL; GLOBE; CONTROL; FUNCTION; COMPLEX; LOGIC; AVOID

Derwent Class: T01

International Patent Class (Main): **G06F-013/00 ; G06F-015/16 ; G06F-015/173 ; G06F-015/80 ; H04L-012/28 ; H04L-012/54 ; H04L-012/58**
International Patent Class (Additional): **H04L-012/56**
File Segment: EPI
Manual Codes (EPI/S-X): T01-M02A1

37/9/25 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011130687 **Image available**
WPI Acc No: 1997-108611/199710
Related WPI Acc No: 1998-168657
XRPX Acc No: N97-089914

Multi-computer memory access crossbar architecture - has crossbar network to which are connected processing nodes, contg. interfaces that provide routing signals in local registers, and circuits for forming communication paths through crossbar networks in response to routing signals

Patent Assignee: MERCURY COMPUTER SYSTEMS INC (MERC-N)
Inventor: FRISCH R C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5598568	A	19970128	US 9358485	A	19930506	199710	B

Priority Applications (No Type Date): US 9358485 A 19930506
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5598568	A		391	G06F-013/00	

Abstract (Basic): US 5598568 A

A multi-computer is made up of a crossbar network to which are connected processing nodes and I-O interface nodes. The processing nodes include crossbar interface circuits that provide routing signals in local registers so that a local processor can access memory in remote processing nodes. The crossbars include circuits to establish communication paths through the crossbar networks in response to the routing signals, so that a local processor has direct access to remote memory, which is mapped into local address space.

The routing signal can have a broadcast mode and can establish **priority** for the signal. Under some circumstances the crossbar circuit can choose between alternative paths through a crossbar. Arbitrary sized and shaped networks of crossbars can be readily implemented, and the direct memory burst transactions allow very high **speed** performance.

USE/ADVANTAGE - Each processor node directly accesses memory of other processor node. Scalable, high performance multi-computer communication system, in which multiple, direct memory accesses can occur simultaneously. contains reliable standard functional modules.

Dwg.1/3

Title Terms: MULTI; COMPUTER; MEMORY; ACCESS; CROSSBAR; ARCHITECTURE; CROSSBAR; NETWORK; CONNECT; PROCESS; NODE; CONTAIN; INTERFACE; ROUTE; SIGNAL; LOCAL; REGISTER; CIRCUIT; FORMING; COMMUNICATE; PATH; THROUGH; CROSSBAR; NETWORK; RESPOND; ROUTE; SIGNAL
Derwent Class: T01
International Patent Class (Main): G06F-013/00
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-H01; T01-H07C7C; T01-S

37/9/26 (Item 26 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010973621 **Image available**
WPI Acc No: 1996-470570/199647
XRPX Acc No: N96-396799
VC connection method for data communication network - involves sending out band reservation demand to link **positioned in optimum route**
Patent Assignee: CHOKOSOKU NETWORK COMPUTER GIJUTSU KENKY (CHOK-N); COMPUTER TECHNOLOGY LAB (COMP-N); ULTRA-HIGH SPEED NETWORK (ULTR-N)
Inventor: KAKEMIZU M
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8237277	A	19960913	JP 95292609	A	19951110	199647	B
US 5805072	A	19980908	US 95565914	A	19951201	199843	

Priority Applications (No Type Date): JP 94307615 A 19941212
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8237277	A		25	H04L-012/28	
US 5805072	A			G05B-013/02	

Abstract (Basic): JP 8237277 A

The VC connection method involves handling a band reservation demand according to the **hierarchical** structure of the network. The first layer rubber substitute network updates the stored roots that connect the networks of the first layer. The optimum route is determined for a given demand.

The band reservation demand to the **link positioned** on that optimum route is sent out. The band reservation is performed by the exchange node of both ends of the link on the selected optimum route.

ADVANTAGE - Improves band reservation **speed** . Increases band reservation processing efficiency. Extracts rubber substitute network manager of necessary higher order quickly and correctly. Prevents loss of reservation call. Improves route selection efficiency. Raises band utilisation efficiency. Increases reliability. Simplifies exchange node structure. Reduces processing load of sub network manager. Shortens band release processing time.

Dwg.1/8
Title Terms: CONNECT; METHOD; DATA; COMMUNICATE; NETWORK; SEND; BAND; RESERVE; DEMAND; LINK; **POSITION** ; OPTIMUM; ROUTE
Index Terms/Additional Words: VIRTUAL; CHANNEL
Derwent Class: W01
International Patent Class (Main): G05B-013/02; **H04L-012/28**
International Patent Class (Additional): H04J-003/24; H04L-012/50; H04L-012/56; H04M-003/00; H04Q-003/00
File Segment: EPI
Manual Codes (EPI/S-X): W01-A03B; W01-A06E1; W01-A06E2B; W01-A06G2; W01-C02A7

37/9/27 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010932564 **Image available**
WPI Acc No: 1996-429514/199643

XRPX Acc No: N96-361879
High speed **microcontroller system for low operational** speed **peripheral equipment - generates integral multiple clock signal based on which wait signal in output by wait mediation circuit**
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8212159	A	19960820	JP 9518175	A	19950206	199643	B

Priority Applications (No Type Date): JP 9518175 A 19950206
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8212159	A		9	G06F-013/42	

Abstract (Basic): JP 8212159 A

The microcontroller system includes a clock signal generator circuit (12) **positioned** in a microcontroller (1). Several peripheral devices (2-1 to 2-n) are connected to this microcontroller. At least one of the peripheral devices has a waiting function and generates a waiting signal. The microcontroller detects and accesses the address assigned to the peripheral equipment which needs a wait operation.

An automatic wait signal for predetermined time is generated. When the wait signal is input, the automatic wait signal circuit (13) is controlled to perform the wait operation. An intermediate signal generator circuit (16) generates a clock signal that is integral multiple of the clock signal during this wait operation mode. Based on this clock signal, a wait mediation circuit (21) generates a wait signal.

ADVANTAGE - Improves system configuration flexibility. Assures adequate system **speed** . Secures high performance.

Dwg.1/10

Title Terms: HIGH; **SPEED** ; SYSTEM; LOW; OPERATE; **SPEED** ; PERIPHERAL; EQUIPMENT; GENERATE; INTEGRAL; MULTIPLE; CLOCK; SIGNAL; BASED; WAIT; SIGNAL; OUTPUT; WAIT; CIRCUIT
Derwent Class: T01
International Patent Class (Main): G06F-013/42
International Patent Class (Additional): G06F-001/06; G06F-012/00; G06F-013/14
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-H05B; T01-K

37/9/28 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010814382 **Image available**
WPI Acc No: 1996-311335/199632
XRPX Acc No: N96-261647
Input-output interface to computer with controlled data transfer speed **- has bus connection controller coupled to reference clock controlled by rate controller with queues to determine execution sequence**
Patent Assignee: NEC CORP (NIDE)
Inventor: SUGIMOTO K
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2728364	A1	19960621	FR 9515086	A	19951219	199632	B
JP 8171526	A	19960702	JP 94315242	A	19941219	199636	

US 5784647 A 19980721 US 95575119 A 19951219 199836

Priority Applications (No Type Date): JP 94315242 A 19941219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2728364	A1		51	G06F-013/368	
JP 8171526	A		11	G06F-013/10	
US 5784647	A			G06F-013/18	

Abstract (Basic): FR 2728364 A

The input-output interface connects to the input-output bus (5) of a server (1). The input-output interface is connected via a data bus to a memory block. The interface is connected to a reference clock generator (2).

The interface has a bus interface controller (32), coupled via the input-output bus to the server, to receive input-output requests. An input-output controller (34) is coupled to the bus interface controller and to the memory block. A transfer rate controller is connected to the interface controller. The rate controller has a queue management section holding requests for input-output access, a **priority** file, an instance queue and an execution queue.

ADVANTAGE - Provides direct access to memory for controlled sequential data transfer. Memory interface ensures data transfer is constant rate to give precise reading needed for correct transfer of video or audio data. Ensures data transfer is within externally imposed time window.

+

Dwg.2/9

Title Terms: INPUT; OUTPUT; INTERFACE; COMPUTER; CONTROL; DATA; TRANSFER; **SPEED** ; BUS; CONNECT; CONTROL; COUPLE; REFERENCE; CLOCK; CONTROL; RATE; CONTROL; QUEUE; DETERMINE; EXECUTE; SEQUENCE
Derwent Class: T01; T03
International Patent Class (Main): G06F-013/10; G06F-013/18; G06F-013/368
International Patent Class (Additional): G11B-020/10
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-H05B3

37/9/29 (Item 29 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010780341 **Image available**
WPI Acc No: 1996-277294/199628
Related WPI Acc No: 1993-216044
XRPX Acc No: N96-233325

Interface chip for voice processor - receives requests from two processors and coordinates data flow between them

Patent Assignee: DICTAPHONE CORP (DICT)
Inventor: DALY D F; DWYER J J; GRANDY T C; HARRIS M N; MORLANDO S J; SEKAS M; SHARMA S V
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5524261	A	19960604	US 91816516	A	19911231	199628	B
			US 93102527	A	19930805		
			US 94329795	A	19941026		

Priority Applications (No Type Date): US 91816516 A 19911231; US 93102527 A 19930805; US 94329795 A 19941026
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5524261	A		9	G06F-013/14	Cont of application US 91816516 Cont of application US 93102527

Abstract (Basic): US 5524261 A

The voice processor interface chip has an arbitration unit (16) for setting a higher **priority** to the voice data, being sent to and from a personal computer processor via a bus, than to data on a second bus. Two interface units (12,26) in communication with the arbitration unit, have a **number** of communication **ports** for communicating with resp. the first and second buses.

A control register (14), in communication with the interface units and with the arbitration unit, provides control for defining communication character addresses. A RAM interface (20), in communication with the arbitration unit, stores data including the voice data and exchanges commands and status so that the processor and the pc processor can directly access the RAM interface with random access addressing. A clock is connected between and communicates with the arbitration unit and the RAM interface.

USE/ADVANTAGE - Can receives requests from two processors and coordinates data flow. Provides high integration and low package density.

Dwg.1/5

Title Terms: INTERFACE; CHIP; VOICE; PROCESSOR; RECEIVE; REQUEST; TWO; PROCESSOR; COORDINATE; DATA; FLOW
Derwent Class: T01; U13; W01
International Patent Class (Main): G06F-013/14
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-C08A

37/9/30 (Item 30 from file: 350)

010743945 **Image available**
WPI Acc No: 1996-240900/199625
XRPX Acc No: N96-201635

Data processing appts. with CPU for data and BCU for data control - extends wait state during read access request to external device immediately before clock change point when CPU inputs data corresp. to read access request until data is established on internal bus

Patent Assignee: NEC CORP (NIDE)
Inventor: SUGIMOTO H
Number of Countries: 005 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 713170	A1	19960522	EP 95118158	A	19951117	199625	B
JP 8147161	A	19960607	JP 94311200	A	19941121	199633	
US 5850541	A	19981215	US 95561332	A	19951121	199906	
			US 97790805	A	19970130		

Priority Applications (No Type Date): JP 94311200 A 19941121
Cited Patents: EP 432575; EP 579369; EP 624837
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 713170	A1	E	17	G06F-001/32	
Designated States (Regional): DE FR GB					
JP 8147161	A		14	G06F-009/30	
US 5850541	A			G06F-001/04	Cont of application US 95561332

Abstract (Basic): EP 713170 A

The data processing appts. includes a CPU section (101) for operating on data and a BCU section (105) for controlling data inputs and outputs between the CPU and external devices (107). The BCU is connected to the CPU via an internal bus and to the external devices via an external bus. It generates a bus cycle on the external bus in response to an access request from the CPU and generates wait states during the bus cycle according to the response **speed** of the external device being accessed.

A clock control section **located** in the BCU section supplies an externally supplied clock (110) to the inside of the CPU and BCU sections. During a read access request to the external device from the CPU, the wait state is extended immediately before the change point of the clock when the CPU inputs, via the internal bus, input data corresp. to the read access request, until the data has been established on the internal bus.

USE/ADVANTAGE - In data processing appts. during access to external storage device or peripheral device provides wait control according to response **speed** of device to be accessed.

Reduces amount of power consumed by CPU that requires wait control according to response **speed** of device to be accessed, and prevents processing **speed** of CPU section from decreasing. Eliminates need for wait control function in CPU section.

Dwg.1/10

Title Terms: DATA; PROCESS; APPARATUS; CPU; DATA; DATA; CONTROL; EXTEND; WAIT; STATE; READ; ACCESS; REQUEST; EXTERNAL; DEVICE; IMMEDIATE; CLOCK; CHANGE; POINT; CPU; INPUT; DATA; CORRESPOND; READ; ACCESS; REQUEST; DATA; ESTABLISH; INTERNAL; BUS

Index Terms/Additional Words: CENTRAL; PROCESSING; UNIT; BUS; CONTROL; UNIT

Derwent Class: T01

International Patent Class (Main): G06F-001/04; G06F-001/32; G06F-009/30

International Patent Class (Additional): G06F-013/42

File Segment: EPI

Manual Codes (EPI/S-X): **T01-C07D** ; T01-H07A2; T01-K

37/9/31 (Item 31 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010590443 **Image available**

WPI Acc No: 1996-087396/199609

XRPX Acc No: N96-073335

Personal computer system with alternate controller - has register coupled to local processor bus for receiving and retaining status information regarding which microprocessor and alternate controller accommodated in connector is active

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: HUYNH D Q; LAM K V; TRAN L T

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5485585	A	19960116	US 92947856	A	19920918	199609	B

Priority Applications (No Type Date): US 92947856 A 19920918

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5485585	A		10	G06F-013/00	

Abstract (Basic): US 5485585 A

The system has a high **speed** local processor data bus, an input/output data bus, and a microprocessor coupled directly to the local processor bus. A connector coupled directly to the local processor bus accommodates reception of an alternate system controller. Only one of the microprocessor and an alternate system controller accommodated in the connector functions as an active system controlling processor over any defined interval of time.

A register coupled to the local processor bus receives and retains status information regarding which of the microprocessor and an alternate system controller accommodated in the connector is the active system controlling the processor over any defined interval of time. The register is accessible to the active system controller. A bus interface controller coupled directly to the local processor bus and to the I-O data bus provides communications between the local processor bus and the I-O data bus. The bus interface controller provides control between the microprocessor and an alternate system controller accommodated in the connector for the transferring system.

ADVANTAGE - Has capability for usual system controlling processor to be reset, initialized and then isolated if an alternate system controller is provided for the system. Provision is made for setting a status bit to identify to diagnostic software which microprocessor is functioning as system controlling processor and **location** of processor. Enables efficient functioning of diagnostic software.

Dwg.4/4

Title Terms: PERSON; COMPUTER; SYSTEM; ALTERNATE; CONTROL; REGISTER; COUPLE ; LOCAL; PROCESSOR; BUS; RECEIVE; RETAIN; STATUS; INFORMATION; MICROPROCESSOR; ALTERNATE; CONTROL; ACCOMMODATE; CONNECT; ACTIVE

Derwent Class: T01

International Patent Class (Main): G06F-013/00

File Segment: EPI

Manual Codes (EPI/S-X): **T01-C07D** ; T01-H07A; T01-H07A2; T01-L02; T01-M06A

37/9/32 (Item 32 from file: 350)

010586175 **Image available**

WPI Acc No: 1996-083128/199609

XRPX Acc No: N96-069503

Small computer system interface - includes bridge located **between high** speed **and low** speed **bus, which has buffer that stores input and output data when data is transferred between them**

Patent Assignee: JUKI CORP (TOLB)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7334281	A	19951222	JP 94124137	A	19940607	199609	B

Priority Applications (No Type Date): JP 94124137 A 19940607

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7334281	A		6	G06F-003/00	

Abstract (Basic): JP 7334281 A

The interface mainly comprises a high **speed** bus (11) for comparatively high **speed** target appts., a low **speed** bus (12) for comparatively slow target appts. and a bridge (13).

When transferring data from a hard disk drive (4) connected on the high **speed** bus to a tape drive (5) connected on the low **speed** bus,

the bridge containing a buffer (14) stores the input and output data between them.

USE/ADVANTAGE - For connecting several equipment and performing data transfer between them according to host computer control. Prevents whole bus from being occupied by input and output of low **speed** appts. Performs efficient data transfer.

Dwg.2/7

Title Terms: COMPUTER; SYSTEM; INTERFACE; BRIDGE; **LOCATE** ; HIGH; **SPEED** ; LOW; **SPEED** ; BUS; BUFFER; STORAGE; INPUT; OUTPUT; DATA; DATA; TRANSFER
Derwent Class: T01; W01
International Patent Class (Main): G06F-003/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-C07C; **T01-C07D** ; W01-A06B1; W01-A07H

37/9/33 (Item 33 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010502427 **Image available**
WPI Acc No: 1995-403749/199551
XRPX Acc No: N95-292382

High speed **peripheral bus for small computer system - has printed wiring conductor configured to reduce reflection of signal to acceptable level, with terminals connecting conductor to high** speed **bus configuration**

Patent Assignee: NCR CORP (NATC)
Inventor: CABANISS F W; MOXLEY D C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5467456	A	19951114	US 92899193	A	19920616	199551	B
			US 94311292	A	19940923		

Priority Applications (No Type Date): US 92899193 A 19920616; US 94311292 A 19940923
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5467456	A		6	G06F-013/00	Cont of application US 92899193

Abstract (Basic): US 5467456 A

The bus has a printed wiring board. A printed wiring conductor is **located** on a first surface of the board. A terminal of a first set of terminals connects a first end of the printed wiring conductor to a high **speed** bus signal of the computer system.

A terminal of a second set of terminals connects to a second end of the printed wiring conductor.

A terminal of a third set of terminals is **located** between the terminal of the first set of terminals and the terminal of the second set of terminals connecting the printed wiring conductor at a branch connection. The printed wiring conductor is folded into a serpentine configuration between the terminal of the second set of terminals and a terminal of the third set of terminals. This creates a desired signal path length sufficient to reduce any reflection of the signal to a

level that does not generate a false logic level.

ADVANTAGE - Provides electrical distance between two branches of high **speed** bus in compact form without using coiled-up cables. Provides SCSI or SCSI-2 bus with recommended 0.3 meter distance between branches without bulky coiled up cable. Easy to manufacture and assemble.

Dwg.2/2
Title Terms: HIGH; **SPEED** ; PERIPHERAL; BUS; COMPUTER; SYSTEM; PRINT; WIRE; CONDUCTOR; CONFIGURATION; REDUCE; REFLECT; SIGNAL; ACCEPT; LEVEL; TERMINAL; CONNECT; CONDUCTOR; HIGH; **SPEED** ; BUS; CONFIGURATION
Index Terms/Additional Words: **HIGH_ SPEED** ; **SPEED** ; PERIPHERAL; BUS; COMPU
Derwent Class: T01
International Patent Class (Additional): G06F-013/40
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-H07A1

37/9/34 (Item 34 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010418907 **Image available**
WPI Acc No: 1995-320222/199541
XRPX Acc No: N95-240917
Data flow control for bus shared by e.g LAN, ATM - using intelligent adaptors between bus and LAN to communicate with central arbiter, which gives highest priority **to those adaptors having nearly fully input buffers containing data for non-full output buffers**
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: METZ W C; RINDOS A J
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5448701	A	19950905	US 92994849	A	19921222	199541	B
JP 6261052	A	19940916	JP 93302093	A	19931201	199541	

Priority Applications (No Type Date): US 92994849 A 19921222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5448701	A		19	G06F-013/36	
JP 6261052	A		16	H04L-012/40	

Abstract (Basic): US 5448701 A

Intelligent adapters connect a number of LAN resources to a bus and a central arbiter decides which adapter has access to the next bus cycle. Each resource has an adapter containing an input buffer for data transmission on to the bus, an output buffer to receive data from the bus and a target register for storing header data. The header data identifies the destination of the block of data in the input buffer.

The adapter has a microprocessor, memory and microcode to assist the buffer to enqueue and dequeue data received into the input and output buffers physically or logically. The adapters communicate to the controller information regarding the fullness and emptiness of the input and output buffers respectively and the contents of the target register through control lines. Using the control information, the controller gives highest **priority** to the adapter having a nearly full input buffer and an empty output buffer of the receiving resource. The next **priority** is given to an nearly empty output buffers with data targeted by an input buffer. The lowest **priority** goes to less than full input buffers targeted to a non-empty output buffer.

USE/ADVANTAGE - In multimedia applications requiring high data transmission **speed** and large bandwidth. Able to accommodate latest information from adapter. Maximises throughput by operating in background of bus. Increase bus cycle to access data and fully utilise buffer. Receiving resources has minimum amount of time in which it has no bus data to process since bus resources that can access bus are

selected based on receiving as well as transmitting resource.
Dwg.2/7
Title Terms: DATA; FLOW; CONTROL; BUS; SHARE; LAN; ATM; INTELLIGENCE; ADAPT ; BUS; LAN; COMMUNICATE; CENTRAL; ARBITER; HIGH; **PRIORITY** ; ADAPT; INPUT ; BUFFER; CONTAIN; DATA; NON; FULL; OUTPUT; BUFFER
Index Terms/Additional Words: DATA; FLOW; CONTROL; BUS; SHARE; LAN; ATM; INTEL
Derwent Class: T01; W01
International Patent Class (Main): G06F-013/36; H04L-012/40
International Patent Class (Additional): G06F-013/38
File Segment: EPI
Manual Codes (EPI/S-X): **T01-C07D** ; T01-H07A2; W01-A03B1; W01-A06B5A; W01-A06E; W01-A06G2

37/9/35 (Item 35 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009401242 **Image available**
WPI Acc No: 1993-094752/199312
XRPX Acc No: N93-072410
Data transmission and processing system with distributed computer nodes - receives data via serial bus linked to acceptance filters, coupled to buffers which connect to specific memory regions.
Patent Assignee: NEC ELECTRONICS GERMANY GMBH (NIDE); NEC CORP (NIDE)
Inventor: TURSKI K
Number of Countries: 017 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4129412	A1	19930318	DE 4129412	A	19910904	199312	B
WO 9305601	A1	19930318	WO 92EP2046	A	19920904	199312	
EP 555456	A1	19930818	EP 92918786	A	19920904	199333	
			WO 92EP2046	A	19920904		
JP 6504172	W	19940512	WO 92EP2046	A	19920904	199423	
			JP 93504960	A	19920904		
DE 4129412	C2	19941027	DE 4129412	A	19910904	199441	
EP 555456	B1	19970423	EP 92918786	A	19920904	199721	
			WO 92EP2046	A	19920904		
DE 59208401	G	19970528	DE 508401	A	19920904	199727	
			EP 92918786	A	19920904		
			WO 92EP2046	A	19920904		
ES 2100361	T3	19970616	EP 92918786	A	19920904	199731	
US 5729755	A	19980317	WO 92EP2046	A	19920904	199818	
			US 9350196	A	19930504		
			US 96629995	A	19960402		

Priority Applications (No Type Date): DE 4129412 A 19910904
Cited Patents: EP 149498; EP 228078; EP 444656; US 4716410
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4129412	A1		8	G06F-013/38	
WO 9305601	A1	G	16	H04L-012/40	
Designated States (National): JP US					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE					
EP 555456	A1	G	2	H04L-012/40	Based on patent WO 9305601
Designated States (Regional): DE ES FR GB IT NL SE					
JP 6504172	W			H04L-012/40	Based on patent WO 9305601
DE 4129412	C2		7	G06F-013/38	
EP 555456	B1	G	10	H04L-012/40	Based on patent WO 9305601

Designated States (Regional): DE ES FR GB IT NL SE

DE	59208401	G	H04L-012/40	Based on patent EP 555456 Based on patent WO 9305601
ES	2100361	T3	H04L-012/40	Based on patent EP 555456
US	5729755	A 8	G06F-015/00	Cont of application WO 92EP2046 Cont of application US 9350196

Abstract (Basic): DE 4129412 A

The data handling system has a **number** of computer **nodes** (N) that are coupled to a data bus (BUS). Each node has a control unit (CC) and main electronic controller (ECU). A control unit has m acceptance filters (AF1-AFm) that contain two 16 bit registers. The 16 bits contain 11 identifier bits and 5 control bits.

The filters connect with receiver buffers (RB1-RBN). Outputs from the buffers **connect** with specific memory **locations** such that specific data regions are defined.

ADVANTAGE - Provides flexible definition of acceptance regions for optimal processing.

Dwg.3/4

Abstract (Equivalent): DE 4129412 C

Data transmissions for installations with distributed calculating nodes or junctions (N) communicating with each other through a serial data bus and exchanging messages.Messages received at a junction are checked, before the head part or identifier is accepted, with the aid of a control unit (CC) and then stored temporarily.

Several acceptance filters (AF1,AF2,AFm) are combined together from a total number of m filters and each combination is assigned to a number n of input buffers (RB).

USE/ADVANTAGE - Data processing systems. load on central unit or station is reduced and efficiency and **speed** of action improved.

Dwg.1/4

Abstract (Equivalent): EP 555456 B

Process for the transmission of data in a data processing system with distributed computing nodes (N) communicating with one another via a serial data bus and between which objects can be exchanged, in which process received objects are tested at a computing node (N) for their acceptance with the aid of a control device (CC) and also temporarily stored and are thereafter stored in a memory (M) allocated to a central processing unit (ECU), characterised by the following steps: a plurality of **hierarchically** arranged acceptance filters (AF1, AF2, AFm) are randomly allocated to a plurality of receiving buffers (RB1, RBn-1, RBn), which in each case are provided to receive more than one object; the full bit width of a head part (identifier) present in an object is tested by the **hierarchically** arranged acceptance filters (AF1, AF2, AFm); an accepted object is temporarily stored in a receiving buffer (RB1, RBn-1, RBn) allocated to the acceptance filters, and the object temporarily stored by the receiving buffer (RB1, RBn-1, RBn) is stored in the memory (M) of the central processing unit (ECU).

Dwg.1/4

Abstract (Equivalent): US 5729755 A

The data handling system has a **number** of computer **nodes** (N) that are coupled to a data bus (BUS). Each node has a control unit (CC) and main electronic controller (ECU). A control unit has m acceptance filters (AF1-AFm) that contain two 16 bit registers. The 16 bits contain 11 identifier bits and 5 control bits.

The filters connect with receiver buffers (RB1-RBN). Outputs from the buffers **connect** with specific memory **locations** such that specific data regions are defined.

ADVANTAGE - Provides flexible definition of acceptance regions for optimal processing.

Dwg.3/4

Title Terms: DATA; TRANSMISSION; PROCESS; SYSTEM; DISTRIBUTE; COMPUTER; NODE; RECEIVE; DATA; SERIAL; BUS; LINK; ACCEPT; FILTER; COUPLE; BUFFER; CONNECT; SPECIFIC; MEMORY; REGION
Index Terms/Additional Words: CAN
Derwent Class: Q17; T01
International Patent Class (Main): **G06F-013/38** ; **G06F-015/00** ; **H04L-012/40**
International Patent Class (Additional): B60R-016/02; **G06F-013/40** ; H04J-003/26
File Segment: EPI; EngPI
Manual Codes (EPI/S-X): T01-H07; T01-M02A

37/9/36 (Item 36 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009280035 **Image available**
WPI Acc No: 1992-407446/199249
XRPX Acc No: N92-310753

Computer ring interconnect system architecture transferring multiple data items concurrently - delays transfer of voucher signals for information of partic. urgency level through node when associated system component is ready to transmit information of higher urgency level

Patent Assignee: APPLE COMPUTER INC (APPY)
Inventor: SWEAZEY P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5165019	A	19921117	US 90530111	A	19900529	199249	B

Priority Applications (No Type Date): US 90530111 A 19900529
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5165019	A		13	G06F-013/38	

Abstract (Basic): US 5165019 A

In a computer system ring interconnection a **number** of **nodes** are connected by transmission appts. to a source node of information and a recipient node of information and associated with at least one of a number of computer system components. Each of the nodes includes appts. to receive and transmit information to and from the associated system component(s) including voucher signal **placing** appts. indicating internodal information for transfer. Voucher signal receive appts. determines the ability to receive. Ticket signal **placing** appts. indicates the ability to receive information associated with the voucher. Appts. relays information to other nodes. The nodes also have internodal relay appts. for tickets and vouchers.

Information selection appts. depending on urgency status includes appts. for storing information originated from component and information from other nodes to other nodes based on urgency level. Appts. selects this information to be transferred on the basis of highest urgency level. Appts. delays the transfer of voucher signals for information of a particular urgency level through a node when the associated system component is ready to transmit information of a higher urgency level.

USE/ADVANTAGE - Secondary interconnection arrangement for computer system capable of handling concurrently information from a number of sources directed to a number of destinations and selecting among information available for handling in a manner that most urgent

information is handled first. Increased load handling abilities of computer system.

Dwg.1/3

Title Terms: COMPUTER; RING; INTERCONNECT; SYSTEM; ARCHITECTURE; TRANSFER; MULTIPLE; DATA; ITEM; CONCURRENT; DELAY; TRANSFER; VOUCHER; SIGNAL; INFORMATION; LEVEL; THROUGH; NODE; ASSOCIATE; SYSTEM; COMPONENT; READY; TRANSMIT; INFORMATION; HIGH; LEVEL

Derwent Class: T01

International Patent Class (Main): G06F-013/38

File Segment: EPI

Manual Codes (EPI/S-X): **T01-C07D** ; T01-H05B; T01-H07A

37/9/37 (Item 37 from file: 347)

DIALOG(R)File 347:JAPIO

05950695 **Image available**

PACKET COMMUNICATION PROCESSING METHOD

PUB. NO.: 10-233795 [JP 10233795 A]

PUBLISHED: September 02, 1998 (19980902)

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APPL. NO.: 09-033551 [JP 9733551]

FILED: February 18, 1997 (19970218)

INTL CLASS: [6] H04L-012/46; **H04L-012/28** ; H04L-012/56

JAPIO CLASS: 44.3 (COMMUNICATION -- Telegraphy)

ABSTRACT

PROBLEM TO BE SOLVED: To permit plural LAN terminals stored in a single subscriber storage node to belong to high-order **hierarchy** groups which mutually differ by describing identifiers showing the physical **connection positions** of the LAN terminals and identifiers showing the high-order **hierarchy** groups to which the LAN terminals belong in a packet heater.

SOLUTION: A CUG identification function 61 receives a MAC frame 51 from an LAN 21. The CUG identification function 61 identifies a CUG **number** from a **port number** receiving the MAC frame 51. Since the MAC frame 51 from the LAN terminals is received by the port of the **port number PORT** 1, for example, the frame is recognized to belong to the MAC-CUG being the high-order **hierarchy** group by using a CUG identification table 62. Thus, the subscriber storage node learns the LAN terminals of the high-order **hierarchy** group to which a packet is to be transferred and suitably selects routing tables generated form each high-order **hierarchy** .

37/9/38 (Item 38 from file: 347)

DIALOG(R)File 347:JAPIO

03453359 **Image available**

HIERARCHICAL PROTOCOL PROCESSING SYSTEM

PUB. NO.: 03-116259 [JP 3116259 A]

PUBLISHED: May 17, 1991 (19910517)

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APPL. NO.: 01-252012 [JP 89252012]
FILED: September 29, 1989 (19890929)
INTL CLASS: [5] **G06F-013/00** ; **H04L-029/06**
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 44.3 (COMMUNICATION -- Telegraphy)
JOURNAL: Section: P, Section No. 1238, Vol. 15, No. 320, Pg. 158, August 15, 1991 (19910815)

ABSTRACT

PURPOSE: To transfer data at a high **speed** by carrying out collectively the data transfer phases of plural layers via a bypass control part.

CONSTITUTION: The connection control parts 1 - 3 covering a layer N through a layer (N + n) are enclosed by a bypass control part 4. The data are taken over by those layers via the part 4. Then the part 4 processes the protocols of the data transfer phases after the **connection** of the highest **rank** layer is set out of plural combinations of layers. Thus the headers of plural layers are collectively added or deleted, and the abnormal data if detected are transferred to the parts 1 - 3 and processed there. Thus the data can be transferred at a high **speed** .